A Microwave Field Effect Transistor Based on Graphene

M. DRAGOMAN[1], G. DELIGEORGIS [2], D. NECULOIU[3],
D. DRAGOMAN[4], G. KONSTANTINIDIS[2], A. CISMARU[1], R. PLANA[5]

[1]National Institute for Research and Development in Microtechnology (IMT), P.O. Box 38-160, 023573 Bucharest, Romania
[2]Foundation for Research & Technology Hellas (FORTH) P.O. BOX 1527, Vassilika Vouton, Heraklion 711 10, Crete, Hellas
3Politehnica University of Bucharest, Electronics Dept., 1-3 Iuliu Maniu Av., 061071 Bucharest, Romania
[4]Univ. Bucharest, Physics Dept., P.O. Box MG-11, 077125 Bucharest, Romania
[5]LAAS CNRS, 7 Avenue du Colonel Roche, 31077 Toulouse Cedex 4, France

Abstract. We present dc and microwave experiments on a graphene-based top-gate field effect transistor. The transistor is acting as an active device far from the Dirac point, and turns into a passive device at the Dirac point, the transistor amplification being suppressed due to lack of carriers. In this way, microwave switches can be implemented based on the specific charge carrier transport in graphene. The maximum stable gain of the transistor is maintained up to 9 GHz, and the mobility of graphene FET is greater than 8000 cm^2/Vs far from the Dirac point.

1. Introduction

Graphene is an atom-thick sheet of graphite consisting of a honeycomb lattice in which carbon atoms bond covalently with their neighbours. The dispersion relation of graphene is linear, and consists of two cones that touch in one point, which is called Dirac point and corresponds to zero energy. The density of carriers in graphene and the Fermi level are tuned by the gate voltage [1]. The microwave graphene FET is a very new transistor [2], [3]. The graphene physical properties such as: (i) ballistic transport at room temperature over a distance of 0.4 μm [3], (ii) intrinsic mobility of carriers of 44 000 $cm^2V^{-1}s^{-1}$ at room temperature [4], and (iii) tunable input impedances around 50 Ω, specific for RF applications, in microwave devices based on graphene [5], make this material a good candidate for very high frequency devices.

The graphene properties are summarized in the Table 1.

Table 1: Graphene properties

Parameter	Value and units	Observations
Mobility	40 000 $cm^2V^{-1}s^{-1}$	At room temperature (intrinsic mobility 200 $cm^2V^{-1}s^{-1}$ in suspended structures)
Mean free path (ballistic transport)	200- 300 nm	At room temperature
Fermi velocity	c/300=1000000 m/s	At room temperature
Thermal conductivity	5000 W/mK	Better thermal conductivity than in most crystals

In the graphene microwave FET, graphene is the channel between the drain (D) and the grounded source (S) contacts. The graphene FET transistor reported below is a top gate FET that has two parallel channels controlled by a single gate electrode (G) to enhance the drain current. The graphene FET is ended by coplanar lines (CPWs), the source electrode is formed from two ground electrodes of the CPWs, while the gate and drain electrodes are the central conductors of the CPWs. The graphene channel is isolated with respect to the top gates by a 200 nm thick PMMA layer. PMMA was selected as gate dielectric due to its high mechanical and thermal stability, high resistivity, of 2×10^6 Ωcm, a similar dielectric constant as SiO_2 (tan $\delta \cong 0.07$ and $\varepsilon_r \cong 3$ at 10 GHz [7]), and easy deposition on a prescribed area.

2. The Fabrication of the Graphene FET

The single-layer graphene sheet was supplied by Graphene Industries and was placed on top of a 300 nm SiO_2 layer that was grown on a high resistivity Si substrate (the resistivity of which is 8 kΩcm) using mechanical exfoliation techniques. The identification of the single layer graphene was done optically and/or using Raman spectroscopy by the company mentioned above. A SEM photo of the microwave FET transistor is presented in Fig. 1.

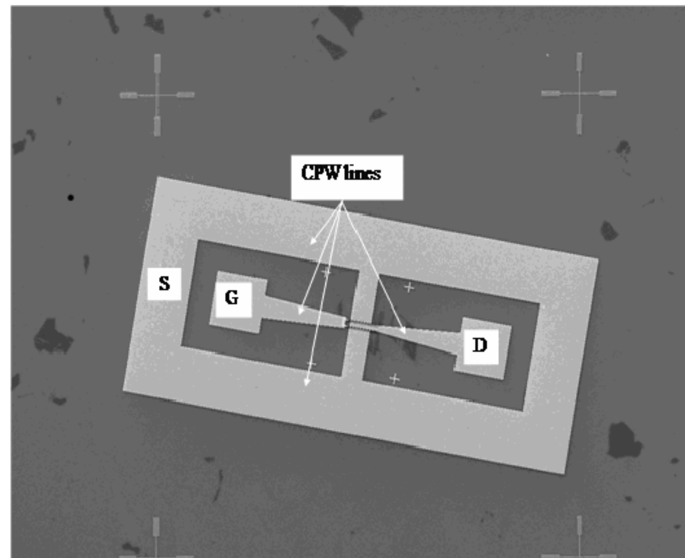
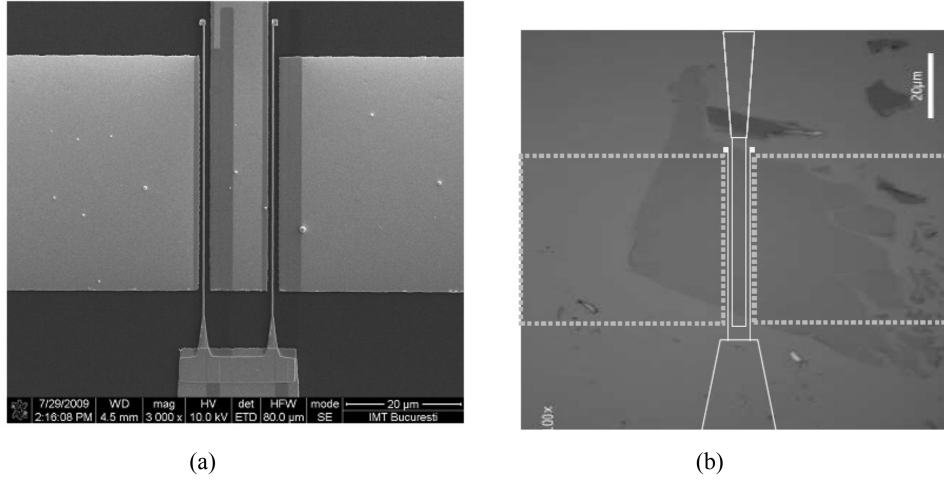


Fig. 1. The microwave graphene FET.

The graphene flake is first identified and mapped in SEM. Then, a set of alignment marks are located near each flake to enable precise alignment of subsequent metallization processes. The alignment marks and the subsequent metallizations were defined using standard e-beam bilayer PMMA lithography. Afterwards, 40 μm wide drain and source electrodes were defined using e-beam. Simultaneously, the CPW electrodes which end the graphene FET were patterned on the substrate. Finally, a 2 nm Ti/300nm Au metallization was evaporated using e-gun, the process being completed by lift-off in acetone. PMMA exhibits an image reversal effect if exposed to high electron doses, and this effect was utilized to get a stabilized PMMA that covers the area where the gate electrode was to be patterned. To complete the device, a fresh PMMA layer was deposited on the sample and a 200 nm thick gate was defined using the e-beam lithography technique. The same metallization, i.e. 2 nm Ti/300 nm Au, was also used to obtain the gate. The process was finalized by lifting off the excess metal in acetone. Acetone does not attack the stabilized PMMA layer during this step, so that the gate electrode can be placed on top of it. A SEM photo of the main area of the graphene FET is presented in Fig. 2. The dimensions of the transistor are: source-drain distance L = 2 μm, gate length L_G = 200 nm, and source/drain width W = 40 μm.



(a) (b)

Fig. 2. (a) SEM photo of the gate area of the graphene microwave FET (b) optical view of graphene with the marked lines of electrodes over it (not scaled).

3. DC and Microwave Characterization of the Graphene FET

We have first measured the dc characteristics of the graphene FET in order to find the Dirac point. The Dirac point displays a kink in the drain current versus drain voltage dependence, I_D–V_D, at a certain drain voltage [8]. Beneath the kink the conduction is unipolar, while at the kink it turns into ambipolar. In the ambipolar regime a pinch-off region travels between source and drain as V_D increases. In Fig. 3a we have displayed the $I_D - V_D$ dependence at $V_G = 2$ V. The kink that characterizes the presence of the Dirac point is located around $V_D = 4$ V. The mobility $\mu = (en)^{-1}(\partial I_D/\partial V_D)\times(L/W)$, where $n = 1.6\times10^{-11}$ cm^{-2} is the carrier concentration, is represented also in Fig. 3a. It can be seen that near the Dirac point the mobility decreases dramatically due to the recombination of carriers, but far from the Dirac point it becomes greater than 8000 cm^2/Vs. The drain current versus gate voltage characteristics, I_D–V_G, is displayed in Fig. 3b for $V_D = 2$ V. At positive gate voltages the charge transport is assumed by electrons, while whole transport takes place at negative gate voltages. The minimum value of the drain current occurs at the gate voltage associated to the Dirac point. In our case, the Dirac point is situated at $V_G = 0$ V. In Fig. 3b we have also shown the transconductance $g_m = \partial I_D / \partial V_G$, which attains a maximum value of 50 µS at a gate voltage of +1 V and has a minimum value of -200 µS around the gate voltage of -2 V. At the Dirac point, *i.e.* at $V_G = 0$ V, the transconductance almost vanishes.

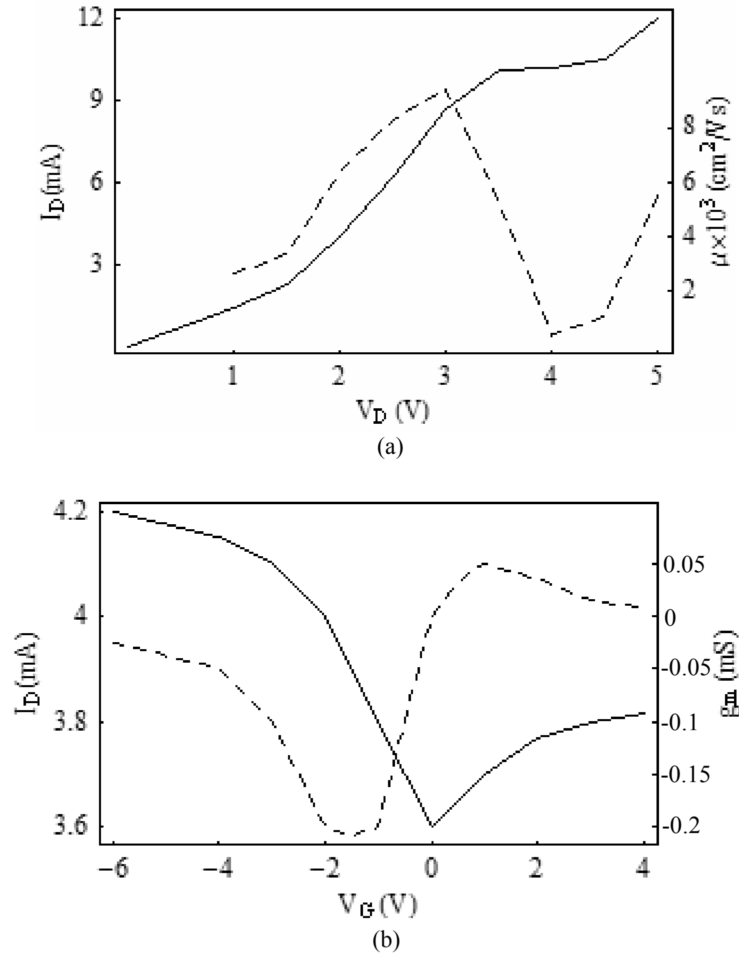


Fig. 3. (a) V_D dependence of I_D (solid line, left vertical axis) and mobility (dashed line, right vertical axis) at $V_G = 2$ V, and (b) V_G dependence of I_D (solid line, left vertical axis) and transconductance (dashed line, right vertical axis) at $V_D = 2$ V.

Working at the Dirac point is undesirable in dc because it worsens the dc parameters: the mobility decreases with orders of magnitude, while the transconductance vanishes and suppresses the FET graphene amplification, producing a quite strong reflection at the gate. However, tuning the drain and gate voltages of the FET graphene near and far from the Dirac point, its gain can be switched OFF and ON. The maximum stable gain, defined as MSG = $|S_{21}|/|S_{12}|$, is around 1 in the OFF state and greater than 1 in the ON state. To demonstrate this switching behavior we have measured the graphene transistor in the microwave spectral region. The measurements of the microwave graphene FET were performed directly on-wafer with a VNA-Anritsu-37397D connected to a

Karl–Suss PM5 on-wafer probe station. The system was calibrated with the SOLT calibration.

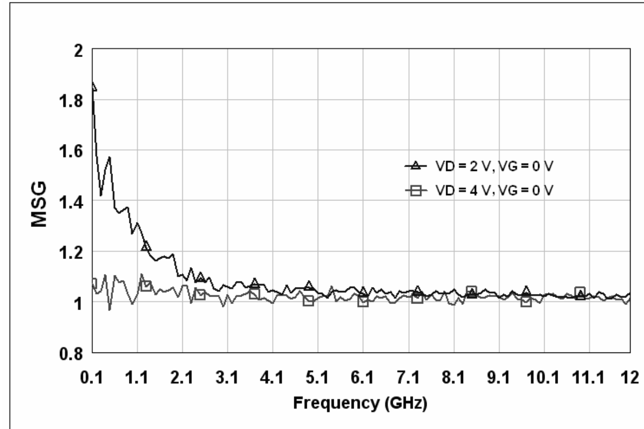


Fig. 4. Frequency dependence of the maximum stable gain at $V_G = 0$ V

In Fig. 4 the maximum stable gain of the microwave graphene FET at $V_G = 0$ is displayed at the drain-source voltages V_D = 2 V and 4 V. Two situations can be inferred from Fig. 4: the transistor behaves as a passive device with a MSG ≅ 1 for V_D = 4 V, i.e. at the Dirac point, and is an active (amplifying) device away from the Dirac point, for instance at V_D = 2 V. The amplification is present also for other drain-source voltages, of 1 V, 6 V and 8 V, but the results are not displayed here.

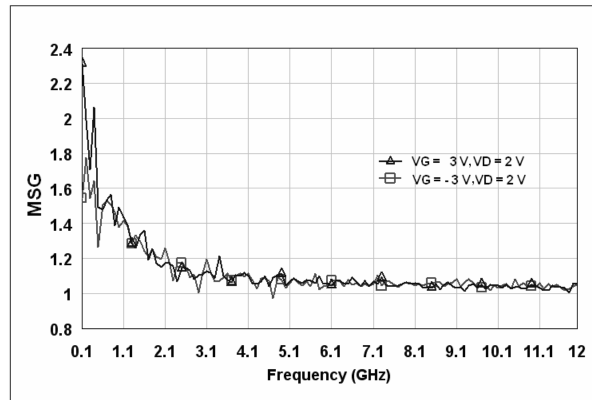


Fig. 5. Frequency dependence of MSG at $V_G \cong -3$ V and $V_G \cong +3$ V.

Far from the Dirac point, the maximum stable gain is almost the same if the polarization is reversed; for example, it is almost the same for $V_G \cong -3$ V and $V_G \cong +3$ V. The corresponding maximum stable gain is displayed in Fig. 5 for $V_D = 2$ V. The graphene transistor amplifies, i.e. has MSG>1, up to 9 GHz. From the results in Fig. 5 it follows that, away from the Dirac point, the microwave behavior of the device does not depend on the polarity of the gate voltage.

4. Conclusion

In conclusion, we have reported a graphene FET, which can switch its state in a reversible way from passive to active, when the drain and gate voltages are varied. This property will be further investigated and will be applied for designing microwave switches that are expected to have good performances taking into account that the switching time is less than 1 ns. Also, the cutoff frequency of the transistor, which is actually around 50 GHz, will be increased in further researches. Recent results [9], [10] have demonstrated that the intrinsic cutoff frequency ($f_c = g_m / 2\pi\, C_{gate}$) of the graphene FETs are exceeding 300 GHz. However, the extrinsic cutoff frequencies where are taken into account the parasitic capacitances ($f_c = g_m / 2\pi\, (C_{gate} + C_p)$) are few GHz and comparable with our results. The graphene FET quest will continue by imposing gate lengths within the ballistic transport limits and the decreasing of the parasitic capacitances.

Reference

[1] NOVOSELOVK.S., GEIM A.K., JIANG D., ZHANG Y., DUBONS S.V., GROGORIEVA I.V., and FIRSOV A.A., *Electric field effect in atomically thin carbon films*, *Science*, **306**, pp. pp. 666–669, 2004.

[2] LIN Y.-M., JENKINS K.A., VLADES-GARCIA A., SMALL J.P., FARMER D B., AND AVOURIS P., *Operation of graphene transistors at gigahertz frequencies*, Nano Letters, **9**, pp. 422–426, 2009.

[3] MERIC I., BAKLITSKAYA N., KIM P., AND SHEPARD K., *RF performances of top-gated, zero-bandgap graphene field-effect transistors*, IEEE Electron Devices Meeting, San Francisco, 15-17 December 2008.

[4] DRAGOMAN M., DRAGOMAN D., DELIGIORGIS G., KONSTANTINIDIS G., NECULOIU D., CISMARU A., and PLANA R., *Current oscillations in wide graphene sheet*, J. Appl. Phys., **106**, p. 044312, 2009.

[5] SHISHIR R.S. and FERRY D.K., *Instrinsic mobility in graphene*, J. Phys.: Condens. Matter., **21**, p. 23204, 2009.

[6] DELIGIORGIS G., DRAGOMAN M., DRAGOMAN D., KONSTANTINIDIS G., NECULOIU D., CISMARU A., AND PLANA R., Microwave propagation in graphene, Appl. Phys. Lett., **95**, p. 073107, 2009.

[7] SUBRAMANYAM G., MATHALA P., CHEVALIER C., DAVIES A., YANEY P., and GROTE J., *Microwave characterization of electro-optic polymers*, MRS Conference Fall, Symposium B, Boston 2002.

[8] MERIC I., HAN M.Y., YOUNG A.F., OZYILMAZ B., KIM P., and SHEPARD K.L., *Current saturation in zero-bandgap, top-gated graphene field-effect transistors*, Nature Nanotechnology, **3**, p. 654, 2008.

[9] LIN W., DIMITRAKOPOULOS C., JENKINS K.A., FARMER D.-B., CHIU H.Y., GRILL A., and AVOURIS P., *100 GHz transistor from wafer-scale epitaxial graphene*, Science **327**, (5966), p. 662, February 2010.

[10] LIAO L., LIN Y.-C., BAO M., CHENG R., BAI J., LIU Y., QU Y., WANG K.L., HUANG Y., DUAN X., *High-speed graphene transistors with a self-aligned gate*,"Nature **467**, pp. 305–308, September 2010.