Design of RF Feedthroughs in Zero-Level Packaging for RF MEMS Implementing TSVs

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Abstract. This paper reports on the design, manufacturing and RF characterization of a zero-level packaging for RF-MEMS devices implementing TSVs (Through-Silicon Via's) and metal bonding. Coplanar interconnection feedthroughs have been modelled and designed for low loss and wideband RF applications. The coplanar slot width of both sides in the vertical interconnection via's pads have been enlarged and reshaped to compensate for the excessive shunt capacitance. Compensated packaged CPW lines have been manufactured and measured in the 0-40GHz frequency band. A significant improvement in terms of RF loss and frequency bandwidth have been obtained thanks to the compensation procedure. A comparison between simulated and measured data up to 40 GHz are presented and discussed.

1. Introduction

Radio Frequency Micro-Electro-Mechanical System (RF-MEMS) devices have demonstrated great potential for applications at millimetre-wave frequencies because of several advantages such as high signal linearity, low insertion loss, and power saving [1]. However, in order to protect its movable friable parts during its entire lifetime, the RF MEMS device needs to be sealed into a hermetic cavity. Several different technologies exist in order to create hermetic cavities [2] and the most of them depends on several factors such as process temperature, device requirements, costs etc,. One of the main approach exists for 0-level packaging is the ―"chip capping". It can be done as die-to-die (D2D) capping, as a die-to-wafer (D2W) capping, or as a wafer-to-wafer (W2W) capping. A capping technology tolerating a certain level of wafer topology is needed. Since the 0-level package

defines the first interface of the RF MEMS device to the outside world, it is clear that the RF design of the package is very important.

The package should provide a good electrical contact for RF signals with the higher level of the system and has a low impact on the RF characterization of the RF structures. The use of low-loss high resistivity cap materials (and MEMS substrate materials) and cap with sufficient cavity height will minimize the degradation influence of the presence of cap [3]. The RF signal feedthrough or transition is one of the promising schemes at 0-level package to serve the RF MEMS devices for wideband interconnection applications [4] . One of the possible implementations for the RF feedthroughs is Vertical via's, implemented either in the MEMS substrate [5,6] or in the Cap [7]. These present a more compact solution (smaller footprint) than the horizontal feedthrough designs, but, the process is more complex as through-wafer hole etching is required. Another advantage of vertical via's is the readiness for 3D implementation.

In this paper, a 0-level package solution based on chip capping is presented. All RF feedthroughs interconnections including Cu-coated through-silicon via's (TSVs) are electromagnetically designed and optimized in order to improve the RF performance of overall structure.

2. Fabrication Process

Within the EU-FP7 project MEMSPACK, a Zero level packaging for RF MEMS devices implementing TSVs and metal bonding is realized using die-to-die bonding process (D2D).

The process flows for the MEMS and cap wafers are manufactured at IMEC (*Interuniversity MicroElectronics Center*). The MEMS package consists of two parts: the MEMS substrate and the CAP. Both are made of high resistivity Si wafers using the 0.35µm CMOS technology adjusted to be compatible with the RF design rules and the flip-chip assembly. This adjustment includes the optimization of the Cu-oxide damascene technology, thicker metal lines and the additional surface passivation layers between the Si and the backend. The CAP wafer was further thinned down to the thickness of 100µm. The thinning step was followed by the etching of the through silicon vias (TSVs) 70µm in diameter. The 2µm thick polymer was then deposited from the back side of the CAP creating the DC and RF isolation for the 5µm thick electroplated copper. As the last step before the assembly the 3µm thick Sn was electroplated to ensure the formation of the reliable solder joints. The CAP and the MEMS dies were then assembled together using the die-to-die (D2D) flip-chip alignment and bonding. The cross-section of the complete assembly is shown in Fig.1 More details on fabrication process including: MEMS substrate, bonding and thining, TSV etching, dielectric patterning, TSV metallization and CuSn/Cu bonding are presented in [8].

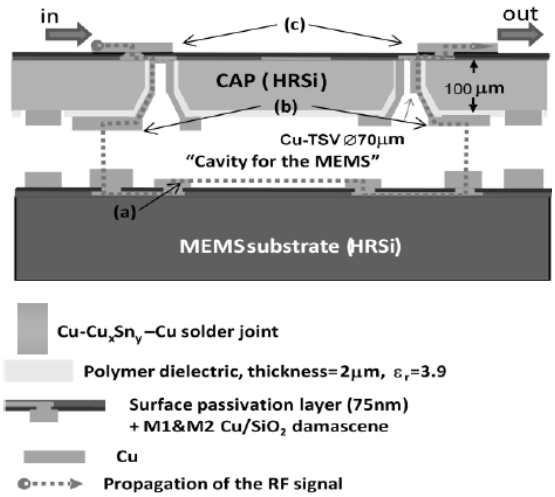

Fig. 1. The cross-section of the hermetic chip MEMS package. The dotted line represents the path for the propagating RF signal.

The blue dotted line in Fig.1 schematically shows the propagation path for the RF signal. The 50Ohm coplanar waveguide (CPW) is patterned on metal of the MEMS die (not shown) and is used to provide the connection between the input and output ports inside the package. The RF signal propagates from the CPW access pad on the top surface of the cap (as show in Fig. 2) through the Cu TSV connected to the short CPW patterned on the back surface of the CAP die. It then continues through the solder joint down to the MEMS die where it goes along the 50 Ohm CPW (which can be replaced by a MEMS in the real application) and then up to the CAP die and to the output RF terminal.

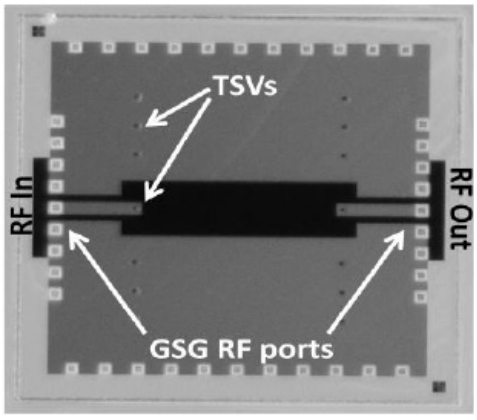

Fig. 9. The top view of the MEMS package with 150μm pitch GWG RF pads.

3. RF Feedthroughs Interconnection Design and Optimization

The most critical part for electrical RF performance is the RF feedthroughs interconnections between layers. In this package, they are based on coplanar-to-coplanar waveguide (CPW-to-CPW) line transitions.
The RF feedthroughs from the MEMS substrate to the RF pads on top of cap consist of the series of three different CPW lines connected through vertical interconnection and Cu TSV. Fig.3 shows the three different CPW lines indicated as (a), (b) and (c) in Fig.1.

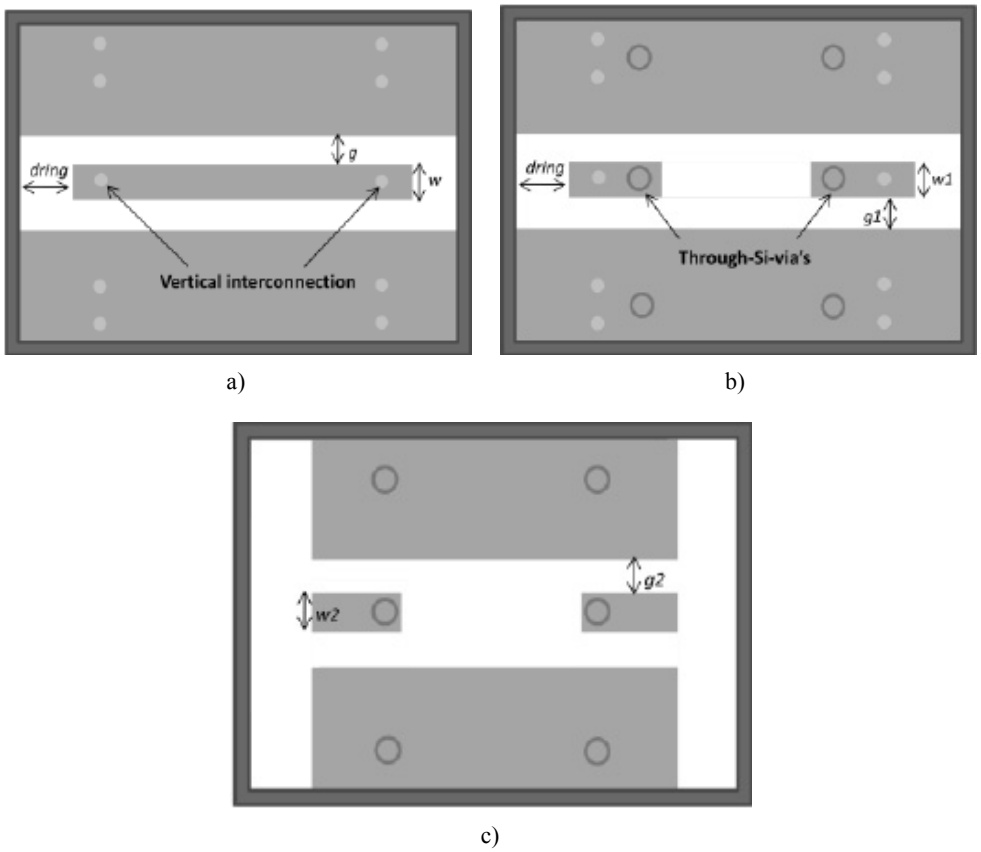

Fig. 3. The three CPW lines with original dimensions before optimization.

A full wave electromagnetic analysis has been performed to study the effect of these transitions on the RF performance, in terms of return and insertion losses. First simple straight CPW-CPW interconnections as indicated in Fig. 3 have been simulated. The dimensions of the three CPW lines are summarized in Table. 1

Table 1. Dimensions of CPW lines

Parameter	Size	Parameter	Size
w	90 µm	*w1*	160 µm
g	50 µm	*g2*	70 µm
dring	100 µm	*w2*	90 µm
Rw (width of ring)	50 µm	*g2*	45 µm

All simulations have been performed using the Ansoft HFSS software. Fig.4 shows the RF performance for these transitions which is significantly deteriorated by the vertical interconnections. Return loss better than 14 dB and insertion loss better than 0.7 dB up to 20 GHz have been obtained.

The basic effects at the transitions of vertical interconnections can be represented as a series reactance. This reactance results from the superposition of capacitive and inductive effects. The capacitive part is caused by dielectric loading at the transition due to the silicon substrate. The inductive contribution is due to the change in current density distribution and direction when going from layer to another layer.

The parameters affecting the interconnection performance are:

- Via diameter.
- Via height (*i.e.* substrate thickness)
- Via pad area (length and width).
- CPW slot width in correspondence of transitions.

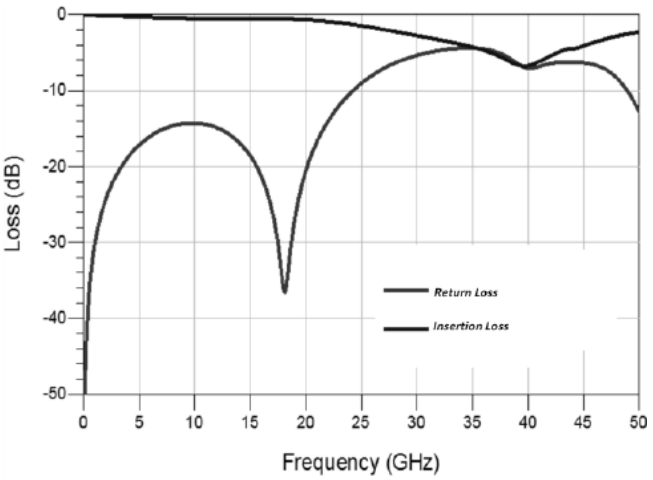

Fig. 4. The three CPW lines with original dimensions before optimization.

The via diameter and height are fixed by technology, the via pad area has been taken as small as possible. We have concentrated on the forth parameter.

In order to improve the RF performance, the basic idea is to compensate the excessive shunt capacitance at the transition by redesigning and adding an inductive section in correspondence of the vertical via. This can be done by locally enlarging the coplanar slot width of the CPW line of both sides in the vertical interconnection pad region as shown in Fig. 5.

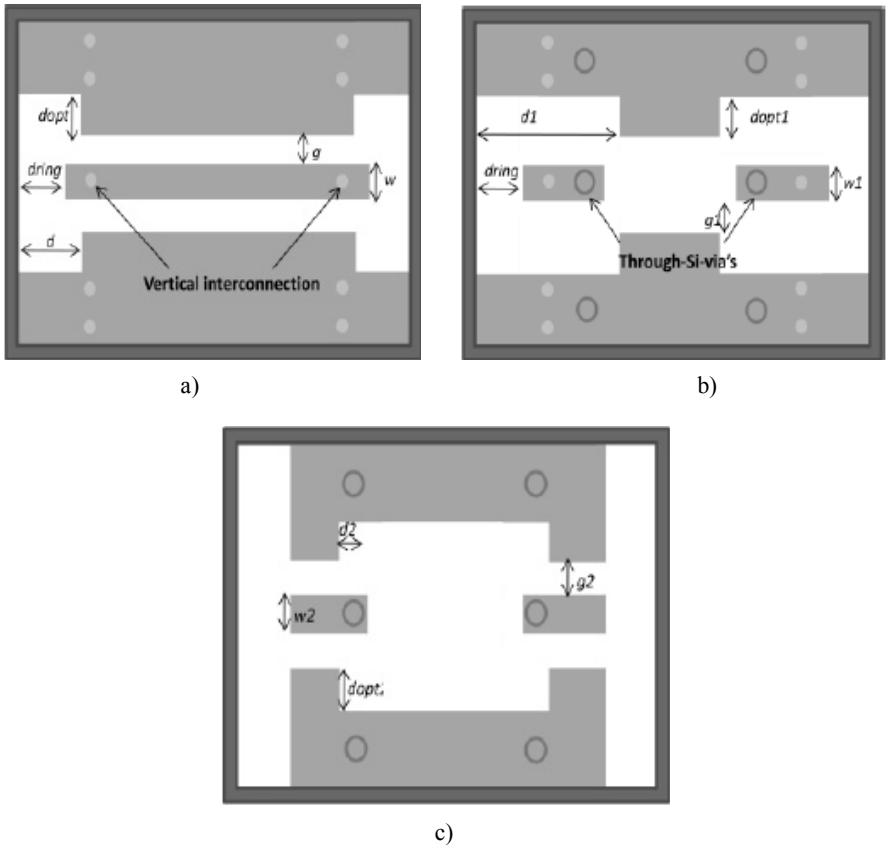

Fig. 5. The three CPW lines dimensions after optimization.

The compensation has been performed by fixing *dring, d, d1, d2* and varying the distances called *dopt, dopt1,dopt2* from 60 µm to 150 µm. The new dimensions for the compensation steps are summarized in Table. 2

Table 2. Dimensions of redesigned parameters

Parameter	Size	Parameter	Size
d	90 µm	*dopt*	60, 90, 120, 140, 150 µm
d1	50 µm	*dopt 1*	60, 90, 120, 150µm
d2	100 µm	*dopt 2*	60, 90, 120 µm

A parametric electromagnetic simulation using Ansoft HFSS is run in order to find the values of *dopt, dopt1, dopt2* which compensate the excessive shunt capacitance and give better RF performance.

The corresponding results are plotted in Fig. 6 and Fig. 7. It can be noted that the increase of *dopt, dopt1, dopt2* leads to an improvement in RF performance.

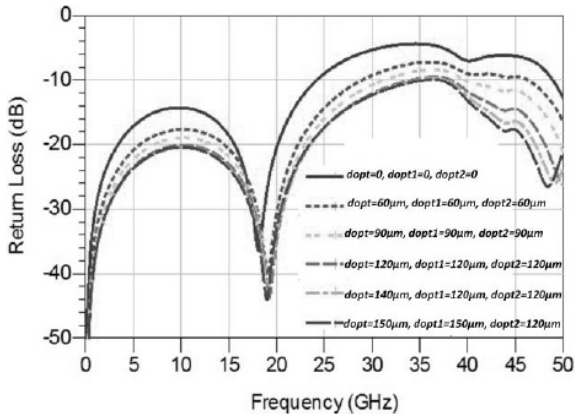

Fig. 6. The simulated Return loss of the compensated structure.

The best return and insertion loss have been obtained for *dopt*=140μm, *dopt1*=120μm, *dopt2*=120μm (green curve). Return loss better than 20 dB and insertion loss better than 0.6 dB from Dc up to 20 GHz have been achieved.

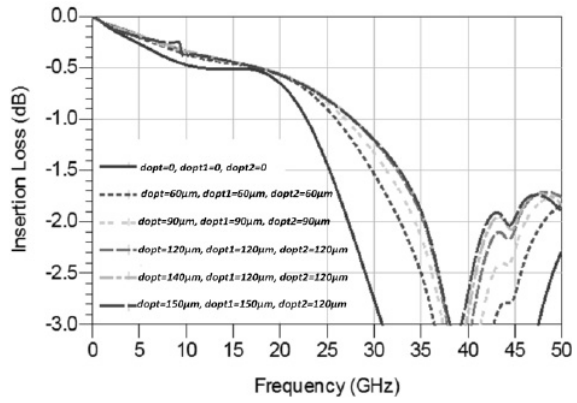

Fig. 7. The simulated Insertion loss of the compensated structure.

Finally, the comparison between the simulated and the measured RF performance of the package in the frequency range of 100MHz-40GHz is shown in Fig. 8 and Fig. 9.

Figure 8 shows that the return loss of both have similar slope but with discrepancy at frequencies less than 20 GHz. The acceptable magnitude of the return loss (better than15dB) indicates that the actual wave impedance of the line is close to the target value in a wide frequency range and that the precision of the flip-chip assembly is accurate enough.

However, a high insertion loss (more than 3.5 dB), indicates the presence of a source of an extra RF loss in the interconnects of the package.

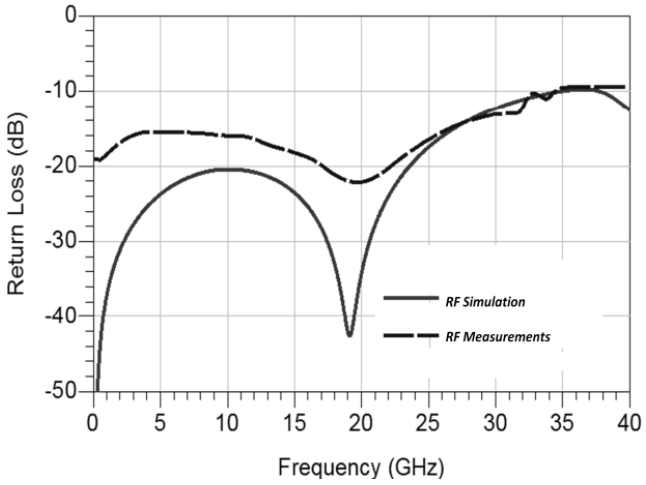

Fig. 8. Comparison between simulated and measured Return loss for the compensated structure.

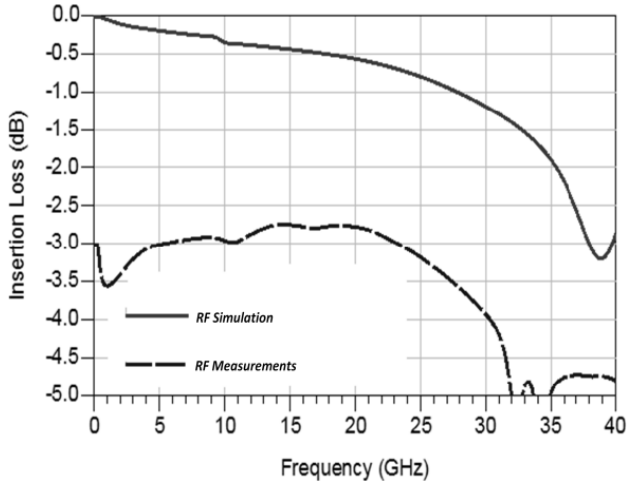

Fig. 9. Comparison between simulated and measured Insertion loss for the compensated structure.

Such abnormal frequency behavior is, however, often reported for coplanar waveguides patterned on a Si substrate [9].

The magnitude of the RF loss in the frequency independent plateau can vary with the doping level of Si and with the surface passivation technique being utilized. Thus, the relatively high level of insertion loss reported in this work may be attributed to the lack of the passivation of the bottom surface (the side from which the TSV are etched) of the HRSi Cap. By minimizing the length of the interconnects (by design) on the Si surfaces, which cannot be passivated, or, by tuning the technology, the insertion loss of the 1-2mm package can be lowered to acceptable values of 0.5-0.7dB.

4. Conclusion

This paper has presented the RF design, manufacturing and characterization of a zero-level packaging for RF MEMS devices implementing TSVs and metal bonding. The CPW to CPW line transitions have been redesigned and optimized in order to compensate the excessive shunt capacitance and improve the RF performance. A simulated return loss better than 20 dB and insertion loss better than 0.6 dB up to 20 GHz have been achieved. A disagreement between measured and simulated loss has been noted due to, most likely, the lack of the passivation of the bottom surface (the side from which the TSV are etched) of the HRSi Cap. The improvement of technology will lead to an acceptable measured loss similar to the simulated one.

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