

# Millimeter Wave CRLH CPW Band-Pass Filter on Silicon and Ceramic Substrate

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**Abstract.** This work deals with the development of a Composite Right / Left Handed (CRLH) band-pass filter (BPF) structure in the millimeter-wave range, working at 40 GHz. The design consists of CRLH artificial lines in a coplanar waveguide configuration (CPW) exhibiting metamaterial properties. Two substrates were used for the fabrication of the BPF structure. The device was firstly processed on a 0.5 mm thick silicon substrate with a 2000 Å Au / 500 Å Cr metallization layer. The silicon substrate offers the possibility of future integration in complex mm-wave circuits. The second substrate used was a super-aluminous ceramic substrate of 0.6 mm thickness. A first layer of 800 Å Ti was deposited, followed by a 4000 Å Au layer. The structures were measured and the results analyzed.

## 1. Introduction

The Composite Right/Left Handed (CRLH) transmission line is an artificial transmission line with metamaterial behavior, made up of series connected capacitances and parallel short ended inductances.

Taking advantage of the dual frequency response of CRLH structures, cf. [1], various types of devices, operating in the microwave frequency range have been developed, on copper plated substrates. Chebyshev band-pass and band-stop filters [2], filters with a dual-band filtering behavior at two arbitrary frequencies [3], dual-band-pass coplanar waveguide configuration filters [4], filters using capacitive-coupled or split ring resonators [5]-[7] and a lot of other constructions were reported.

This paper describes the design (done in IE3D-Zeland), fabrication and measurement of a millimeter wave (MMW) BPF structure.

The device was designed as a CRLH structure in CPW configuration, using series interdigital capacitors and short ended transmission lines as inductors.

Two substrates were used in the manufacturing process: a silicon substrate with a dielectric constant  $\epsilon_{r, Si} = 11.9$  and a resistivity  $\rho = 5 \text{ k}\Omega\cdot\text{cm}$  with a  $1\mu\text{m}$   $\text{SiO}_2$  layer grown through thermal oxidation ( $\epsilon_{r, \text{SiO}_2} = 4.7$ ) and a super-aluminous ceramic substrate with a dielectric constant  $\epsilon_{r, \text{ceramic}} = 9.6$ .

## 2. Overview

The layout of the CPW CRLH elementary cell used in this design is shown in Fig. 1. The cell is composed of two series connected interdigitated capacitors and a ground connected CPW line as inductor.

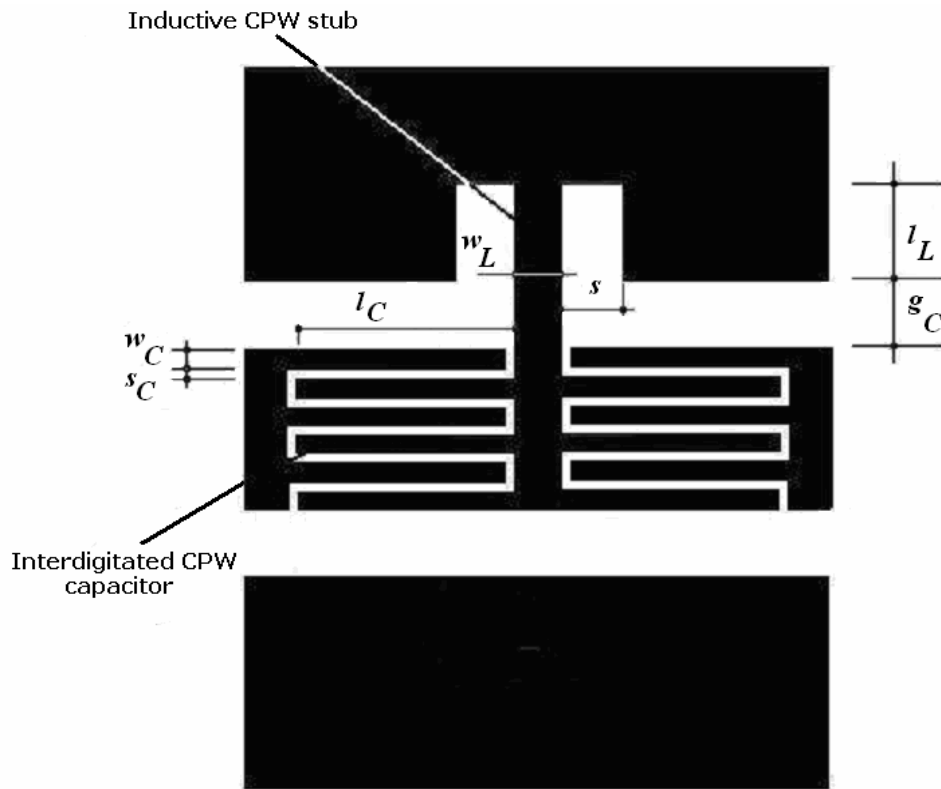
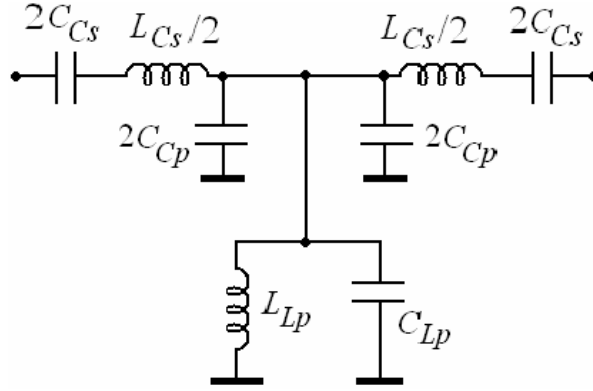


Fig. 1. Layout of the CPW CRLH elementary cell.

The equivalent circuit of the CRLH cell is given in Fig.2 where  $2C_{Cs}$ ,  $L_{Cs}/2$ , and  $2C_{Cp}$  are the capacitance, inductance and the equivalent parasitic capacitance of the interdigitated capacitor, respectively. The equivalent inductance and parasitic capacitance of the inductive grounded line are  $L_{Lp}$  and  $C_{Lp}$ , respectively.



**Fig. 2.** CRLH cell equivalent circuit consisting of the series interdigitated capacitor and of the ground connected inductor.

The two capacitors and the inductive line were designed (cf. [8]) with the purpose of obtaining a series resonance frequency, given by  $C_{Cs}$  and  $L_{Cs}$  equal to the parallel resonance frequency, given by  $L_{Lp}$ ,  $C_{Lp}$  and  $C_{Cp}$ , therefore attaining a balanced structure. The relations for this design are:

$$C_{Cs} = \frac{k}{4\pi f_0 Z_c} \quad (1a)$$

$$L_{Lp} = \frac{k Z_c}{4\pi f_0} \quad (1b)$$

$$C_p = \frac{1}{\pi f_c R H Z_c} = C_{Lp} + 4C_{Cp} \quad (1c)$$

The values of  $C_{Lp}$  and  $L_{Cs}$  were computed for the CRLH structure to be balanced at the frequency  $f_0$  with the formula:

$$L_{Cs} C_{Cs} = L_{Lp} C_p = \frac{1}{(2\pi f_0)^2} \quad (2)$$

It should be remembered that  $f_{c_{LH}} = \frac{1}{4\pi\sqrt{L_{Lp}C_{Cs}}}$  is the cut-off frequency of the LH (Left-Handed) mode and  $f_{c_{RH}} = \frac{1}{\pi\sqrt{L_{Cs}C_p}}$  is the cut-off frequency of the RH (Right-Handed) mode. The introduction of a parameter  $k > 1$  is useful in the design process, in such a way that:

$$f_0 = \sqrt{f_{c_{LH}} \cdot f_{c_{RH}}} = k \cdot f_{c_{LH}} = \frac{f_{c_{RH}}}{k} \quad (3)$$

The minimum and maximum frequencies related to the CRLH frequency bandwidth may be computed as

$$f_{\min} = \frac{f_{c_{RH}}}{2} \left[ \sqrt{1 + \frac{4f_{c_{LH}}}{f_{c_{RH}}} - 1} \right] \quad (4a)$$

and

$$f_{\min} = \frac{f_{c_{RH}}}{2} \left[ \sqrt{1 + \frac{4f_{c_{LH}}}{f_{c_{RH}}} + 1} \right] \quad (4b)$$

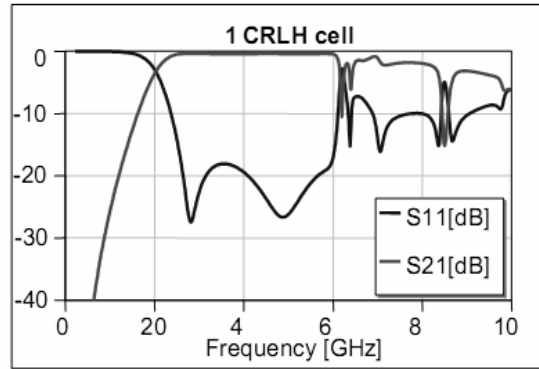
respectively.

Taking into account the substrate thickness, the upper frequency limit was imposed to  $f_{\max} = 75$  GHz. Also, the lower frequency limit was imposed to  $f_{\min} = 20$  GHz. Using the previous relations,  $f_{c_{LH}} = 30$  GHz,  $f_{c_{RH}} = 52$  GHz,  $f_0 \approx 40$  GHz and  $k \approx 1,3$  were computed.

The parallel resonant circuit formed by  $L_{Lp}$  and  $C_{Lp}$  was modeled with an inductive CPW ground connected line with the characteristic line impedance  $Z_{cl} \approx 25 \Omega$ . Computing for  $Z_c = 50 \Omega$ , the following values were obtained:  $2C_{Cs} \approx 106$  fF,  $L_{Cs} \approx 0,3$ nH,  $CC_p \approx 25$  fF,  $L_{Lp} \approx 0,13$  nH,  $C_{Lp} \approx 20$  fF. The resonance of the inductance is:  $f_{0_L} = \frac{1}{2\pi\sqrt{L_{Lp}C_{Lp}}} \cong 97$ GHz (the electrical length at this frequency is  $90^\circ$ ).

The CRLH cell layout was designed such as the length of the interdigitated capacitor be much smaller than the wavelength corresponding to  $f_0$ :  $L_c \ll 2000 \mu\text{m}$  (see Fig. 1). The value  $2C_{Cs} = 106$  fF was obtained for the following geometrical dimensions:  $w_c = 10 \mu\text{m}$ ,  $s_c = 5 \mu\text{m}$ ,  $L_c = 250 \mu\text{m}$  and number of digits equal to 10. For the inductive ground connected line the values obtained were:  $L_L = 277 \mu\text{m}$ ,  $w_L = 42 \mu\text{m}$  and  $s_L = 10 \mu\text{m}$ .

The BPF structure consists of one, two or four series connected CRLH cells. The simulation results for a BPF structure with one CRLH cell having the above computed dimensions are presented in Fig. 3.



**Fig. 3.**  $S_{11}$  and  $S_{21}$  of BPF. Simulated values for one CRLH cell structure on high resistivity silicon substrate.

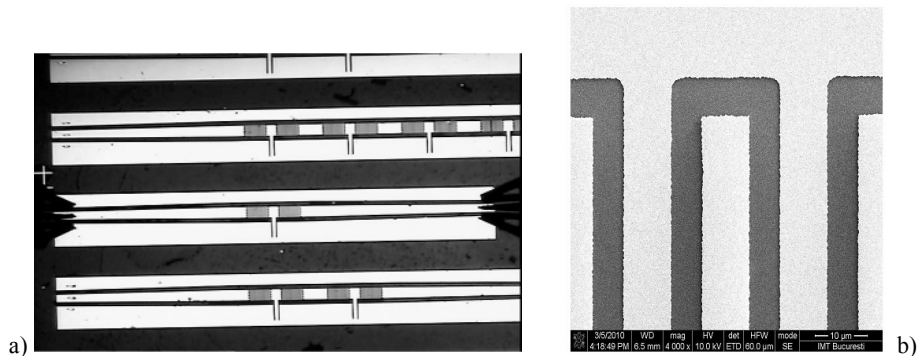
The maximum frequency obtained by simulation (60 GHz) – see Fig. 3 – is lower than the initially imposed one (75 GHz) due to the influence of the substrate thickness on the maximum working frequency of the circuits.

### 3 Experimental Results and Comments

#### A. BPF structures processed on a silicon substrate

The BPF structures were fabricated using standard photolithography. A silicon wafer with 500  $\mu\text{m}$  thickness and 5  $\text{k}\Omega\text{cm}$  resistivity was used as substrate. A 1  $\mu\text{m}$  thick  $\text{SiO}_2$  surface layer was grown on the silicon wafer. The Si wafer was plated through a sputtering process with a metallic layer of 2000  $\text{\AA}$  Au / 500  $\text{\AA}$  Cr.

In Fig. 4 (a) and (b) photos are presented showing the results of the photolithographic process on silicon. Fig. 4 (a) shows band pass filter structures with one, two and four CRLH cells. Fig. 4 (b) presents a detail of the interdigitated capacitor (Scanning Electron Microscopy – SEM – image). Very good line definitions were obtained, with almost no rounding at the corners.



**Fig. 4.** BPF structures on silicon (a) and a detail of an interdigitated capacitor (b).

The electrical measurements on the BPF obtained through photolithography were done with a ANRITSU 37397D Vector Network Analyzer (VNA) with a 110 GHz maximum working frequency combined with a Karl Süss on-wafer characterization equipment. A BPF structure supporting the probe-tips of the on wafer measuring system is shown in Fig.4 (a). The S parameter measurement of a one-cell CRLH BPF structure processed on silicon is given in Fig. 5.

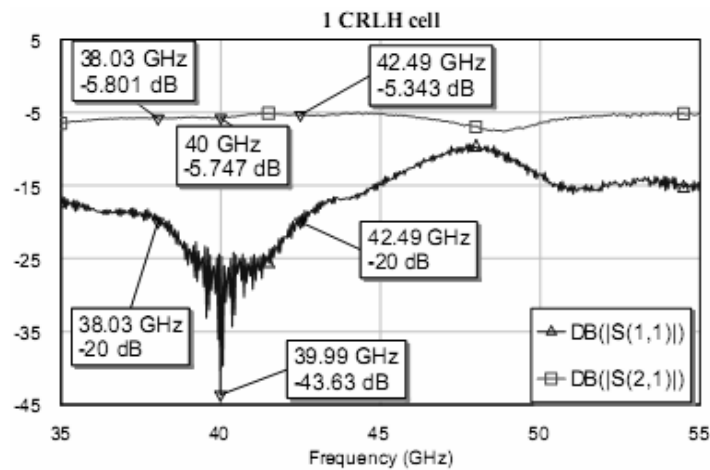


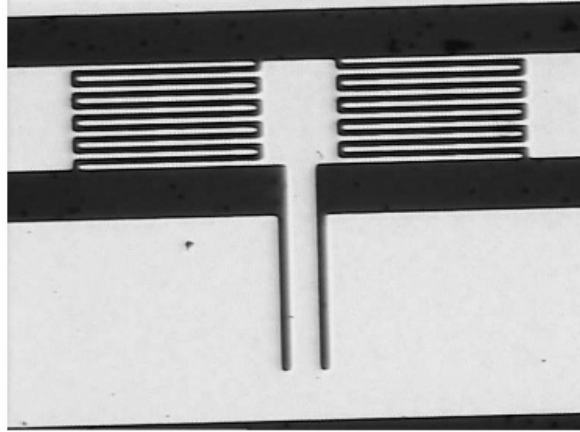
Fig. 5. S11 and S21 parameters of a one CRLH cell BPF structure on silicon.

For one CRLH cell, the S parameter distribution for a frequency scan between 35 GHz and 55 GHz shows a value  $S_{11} < -20$  dB in the frequency range 38 GHz ÷ 42.5 GHz with the maximum value of -43.63 dB at 39.99 GHz. The losses in the same frequency range are about 5-6 dB. The frequency band is 4.5 GHz (for  $S_{11} < -20$ dB).

### ***B. BPF structures processed on a super-aluminous ceramic substrate***

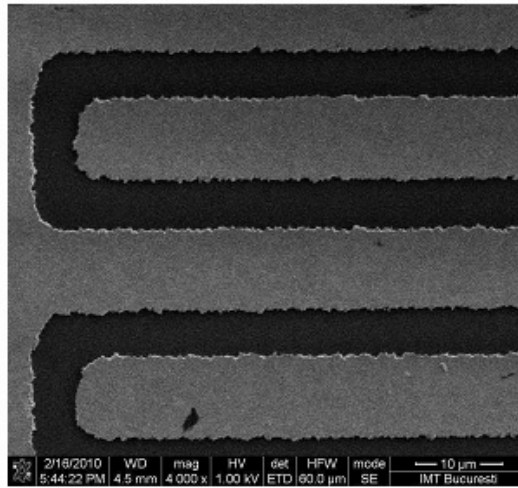
The same structure was processed on a super-aluminous substrate (AlSiMag 614 made by American Lava Corp.) with a dielectric constant  $\epsilon_{r,ceramic} = 9.6$  and a thickness of 0.6 mm. The resistivity can be considered infinite. The process used was the same standard photolithographic process consisting of a one mask exposure / wet etching technique.

An optical microscopy photo is presented in Fig. 6, showing a one CRLH cell BPF structure on ceramic substrate. The interdigital capacitor and the inductive grounded CPW line are visible.



**Fig. 6.** A processed BPF structure on ceramic substrate.

The technological results were not as accurate as was the case for silicon, with a over-etching effect visible in Fig.7. This in turn influenced the values of the capacitance and hence the working frequency of the BPF. The poor results in maintaining the geometrical sizes of the structure processed on ceramic substrate were determined by an imperfect exposure process, due to the slightly curved shape of the ceramic surface.



**Fig. 7.** SEM image of a BPF structure on ceramic substrate: a detail of an interdigitated capacitor.

The measurement of the S parameters was done with the same setup as for the structures on silicon. The results for a one CRLH cell BPF are given in Fig. 8.

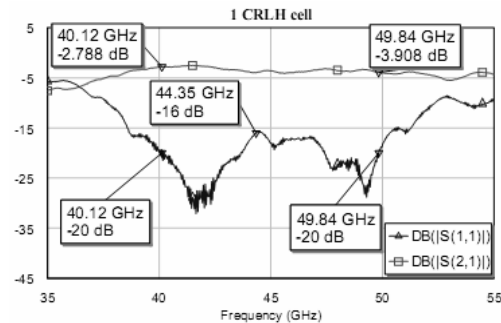


Fig. 8. S parameters of a BPF structure with one CRLH cell on ceramic substrate.

S11 shows a good matching, with values better than -16 dB for a frequency band between 40.12 GHz ÷ 49.84 GHz. The losses are very low in this frequency band with S21 between -2.8 dB ÷ -3.9 dB. This decrease of the losses, in comparison to the silicon case, can be attributed to the practically infinite resistivity of the ceramic substrate. The passband is almost double (9.72 GHz) compared to the structures processed on the silicon substrate.

#### 4. Conclusions

A MMW BPF structure, designed with CRLH-TLs, in CPW configuration is described in this paper. The structure was processed on two different substrates: silicon and alumina ceramic. While the silicon substrate can be easily integrated in more complex millimeter wave circuits, the ceramic substrate showed a much larger frequency band and reduced losses.

Measurements of the BPF structure consisting of one CRLH cell on silicon revealed a 40 GHz working frequency with a 4.5 GHz band. The frequency band for the structures processed on a ceramic substrate was almost 10 GHz. The high losses in the silicon case can be explained due to the low resistivity substrate.

The frequency shift observed for the ceramic substrate is caused mainly by the altered capacitance value due to the over-etching effect.

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