Tapered Walls Via Holes Manufactured Using DRIE Variable Isotropy Process

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Abstract. This paper describes a method to manufacture through wafer via holes with tapered walls for RF applications. The main purpose was the need to obtain via holes with tapered walls that allow depositing seed and barrier layers by Physical Vapor Deposition (PVD) to enable gold electroplating. Method consists in consecutively using of the two basic process types for DRIE technique: isotropic and anisotropic etchings. Thus via holes with 20µm and 100µm diameter having tapered walls with angles between 14° and 18° were manufactured. Thin metal layers were also deposited on the walls by e-beam technique.

1. Introduction

Through wafer via holes manufacturing can be done using different techniques, but Deep Reactive Ion Etching (DRIE) showed its superiority to all other techniques, mainly in respect of pattern transfer accuracy, minimum achievable dimensions and aspect ratio, side effects or wall roughness [1].

The commonly used materials for via holes filling are copper or heavily doped polisilicon, due to their deposition properties [2, 3]. Our aim was to develop this connection type using gold, avoiding in this way problems regarding the resistivity or contamination. Less used as conductive material, method of filling via's by gold electroplating consists in using a sacrificial material as support for the seed layer on the wafer backside and electroplating starting from only one side, without a barrier layer between gold and substrate - as described in [4].

To be able to obtain a continuous seed layer (CrAu) on the walls, we manufactured tapered walls using dry etching with a variable isotropy. We developed this process in such a way to control with a very good precision the angle of the walls. Such a process could be helpful for instance in encapsulation processes, when on devices side small areas are needed, to reduce the chip size, while on the other side contact pads or wire bonding are needed.

2. Manufacturing Method

One of the most important advantages of the DRIE technique for MEMS technology comes from the possibility of using both isotropic and anisotropic etching processes. Moreover, by simply changing of plasma and process parameters (power, gas flow and pressure, substrate bias) it is possible to change the process isotropy during the same run [5-6].

The Bosch type processes, consisting in frequently alternating vertical etching and deposition of protective polymers on the side walls, provide the possibility to obtain an important anisotropy and very high etching rates and this is the main process used in case deep cavities with almost vertical walls are wanted [7]. Isotropic etching, less used, allows to obtain unique structures (mainly as complementary process to the anisotropic one) or to release movable / suspended parts in MEMS devices [6, 8-9].

The complex process developed to achieve the intended purpose, consists in mixing these two processes in the same run in order to obtain tapered walls, allowing the deposition of the seed layer using PVD methods. During manufacturing process alternatively anisotropic and isotropic etching processes are used: anisotropic etching to achieve the depth, while the isotropic etching to enlarge via's on one side in order to obtain the desired angle. Developed method consists in successive anisotropic and isotropic etching cycles, step by step reaching the depth and enlarging via.

To achieve our shape, the passivation polymers deposited on the walls by the Bosch processes have to be removed by a supplementary oxygen plasma cleaning before isotropic etching steps [5].

The main problem of this method remains the dependence of the etching rate on the aspect ratio (ARDE effect–Aspect Ratio Dependent Etching), the usual problem for the DRIE processing. The process needs to be fine tuned for every hole dimension and manufacturing in the same step of via holes with different opening size will be difficult if not impossible.

3. Experimental Results

Manufacturing process starts with thermal oxidation of the wafers, resist deposition and patterning of the via windows (circular holes with 20µm and 100µm diameter) and SiO_2 etching (by RIE) from the holes. Further, both resist and the SiO_2 layer were used as mask for the DRIE process. The tapered via hole process started with a Bosch process. Then, in order to remove the passivation layer deposited over the walls during anisotropic process, an oxygen plasma step was performed. The whole cavity so obtained was enlarged using the isotropic etching process. Without an oxygen plasma step in this process, due to the passivation deposited over the walls in the previous step, internal cavities connected by vertical channels will be obtained, like in [6]. The whole cycle of anisotropic etching /

oxygen plasma / isotropic etching was then repeated until the bottom surface of the wafer was reached. To maintain the desired dimension of the via's on the bottom side of the wafer, as it was patterned on the top side, the whole etching process was completed with an anisotropic etching step.

Three different recipes were tested for the anisotropic etching steps–the characteristics of each one are presented in table 1.

Table 1. Summary of drie anisotropic etching recipes

Recipes (anisotropie etching)	Recipe characteristics	Expected results
1. HER (High Etching Rate)	High gas flow/pressure high power; long etching time.	High etching rate (> 10 μm/min, depending of mask); high roughness due to specific Bosch process profile (scalloping)-up to 1 μm.
2. SDE (Silicon Deep Etch)	Smaller gas flow/pressure and power comparing with HER recipe; substrate bias was increased.	Smaller etching rates (-50% of HER rate) smaller roughness-400…500 nm.
3. LR (Low Roughness)	Gas flow/pressure and power grady reduced comparing with the previous recipes.	Much smaller etching rate (20…25% of HER etching rate); very smooth walls (-30nm).

Isotropic etching steps differ from the previous ones basically by the removal of the passivation gas (C4F8) from the recipe and substrate biasing.

As a first test through silicon via's (TSV) were obtained using HER recipe on 200μm thick silicon wafers (<100> oriented, high resistivity).

Results, presented in figure 1, show that holes were enlarged by about 12μm on each side of the top side, which implies an angle of about 3.8º-the angle was computed considering average tilt angle, taking into account front and bottom side via openings. Wall roughness in this case is in the range of 1μm due to the scalloping, specific to the Bosch process (figure 2.a). Measurements performed showed an etching rate of about 16,6μm/min during anisotropic etching steps (HER recipe), while for the isotropic process etching rate was about 2μm/min.

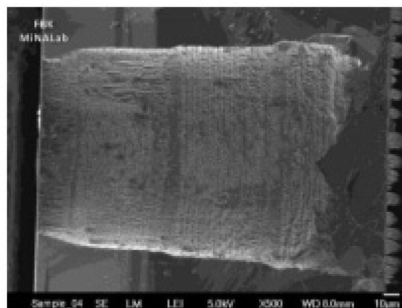


Fig. 1. TSV manufactured using HER recipe.

To reduce the corrugation it was used the procedure proposed by Shikida *et al*. [10] to smooth the asperity by wet etching- but KOH etching solution was replaced with a TMAH one - 25% at 74ºC for 10 minutes (figure 2.b).

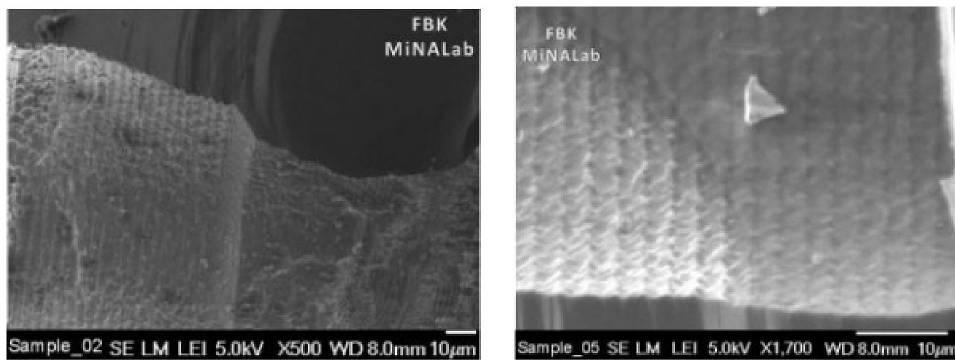


Fig. 2. Scalloping–due to the Bosch effect after via hole manufacturing (a) and after 10min selective corrugation removal in TMAH 25% (b).

Finally, Cr/Au barrier and seed layers were deposited inside the manufactured TSV's - results are presented in figure 3. As we can see, although the corrugation was reduced by wet etching, at the bottom side of the via's there are still some problems due to the walls roughness, deposited layers are not continuous also due to the small angles.

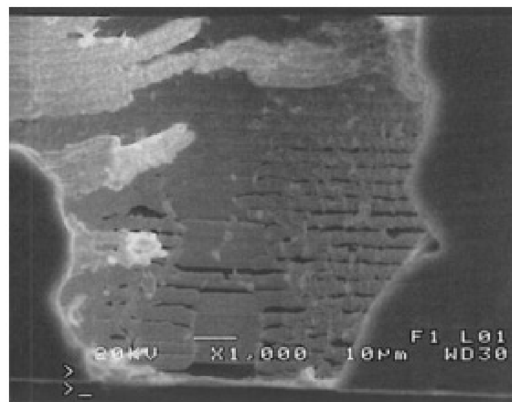


Fig. 3. Seed layer (Cr/Au, 5/150nm).

Since the etching rates strongly depend on the used mask, results obtained were used for a rough estimation of the etching rates for the next experiments with holes dimension. SDE and LR anisotropic recipes were used for tapered via manufacturing, the target being angles of about 20°. Two different hole dimensions

(20µm and 100µm) were used to reach 200microns depth on 500µm thick silicon wafers (<100> oriented wafers); process used involves five anisotropic and four isotropic etching steps for each recipe.

Figures 4-5 present the results obtained for holes with 100µm initial diameter using SDE or LR recipes for anisotropic etching. Measurements performed showed for first recipe an enlargement of the holes of about 50µm on each side for a depth of 195µm, which means an angle of about 14.4º (14.28º ÷ 14.52). For the second recipe (LR), obtained angle was of about 18º (17.74º ÷ 18.04º), but in this case the etching depth was 159µm and the lateral etching was (due to the isotropic etching) in the same range.

For the holes with the second diameter, 20µm, due to the ARDE effect all etching rates are smaller–in this case etching depths were about 128µm when SDE recipe was used, while for the LR recipe was of about 110µm.

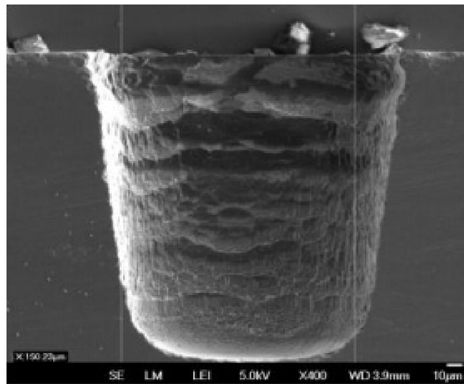


Fig. 4. Via performed using SDE recipe, 100µm diameter.

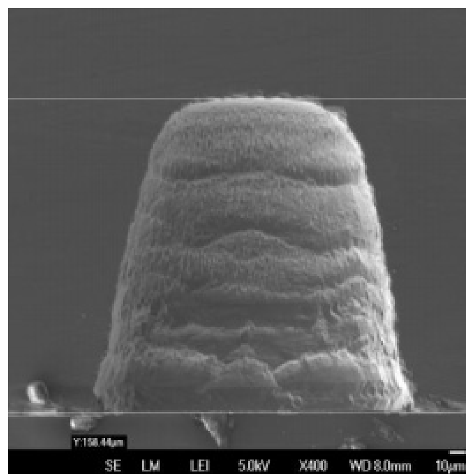


Fig. 5. Via performed using LR recipe, 100µm diameter.

In both cases isotropic etching provided an enlargement of the holes of about 30µm, so that the obtained wall angles were of about 15º for SDE recipe and 17.25º for LR recipe–figures 6 and 7.

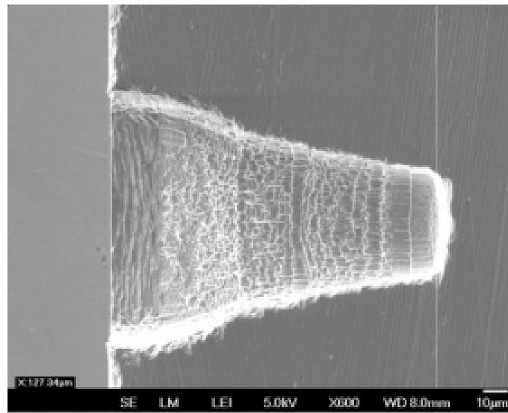


Fig. 6. Via performed using SDE recipe, 20µm diameter.

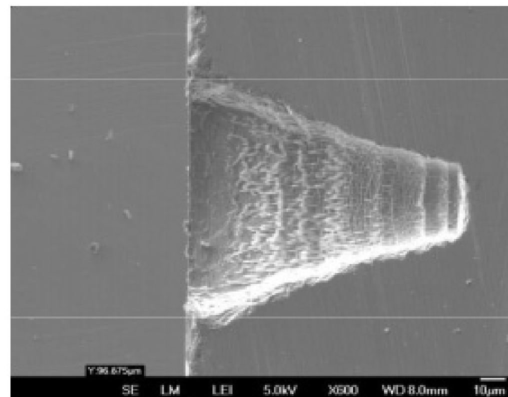


Fig. 7. Via performed using LR recipe, 20µm diameter.

Figures 4-7 show that the walls roughness was reduced–we can assume that this was not only the effect of changing the anisotropic etching recipe (LR and SDE recipes instead HER), but also due to longer isotropic etchings to obtain higher angles (having a polishing effect over the surfaces). Using low roughness recipes (LR and SDE) we can observe the appearance of nanometer peaks on the walls – more evident for 20µm diameter holes and bigger for LR recipe. One method to remove these peaks is to increase the temperature during DRIE processing [11], but this method lead to increasing the etching rate of resist layer used as mask. Finally,

a small bowing effect can be seen in these cases, missing when HER recipe was used.

Structures obtained by using LR recipe were used to deposit barrier and seed layers (Cr/Au, 5/100nm) by e-beam, to verify the quality of these layers - figures 8 and 9.

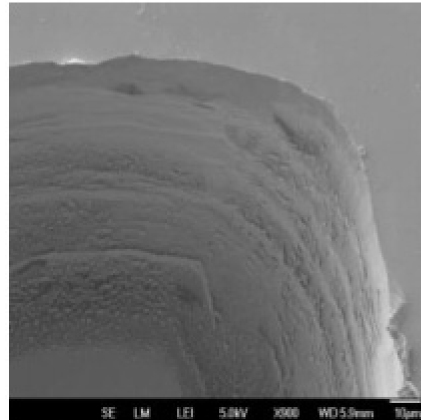
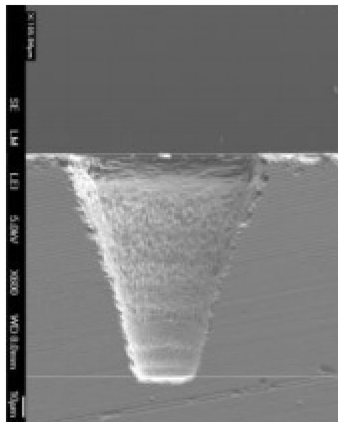
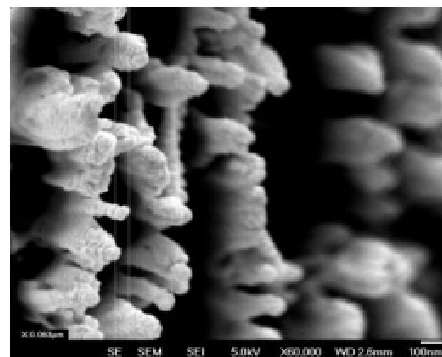


Fig. 8. 100μm diameter via, after seed layer deposition (top view).





a) b)

Fig. 9. 20μm diameter via, after seed layer deposition – cross section (a) and detail of the nanometer peaks (b).

Figures 8 and 9 show that the seed layer was continuously deposited over the walls, providing better coverage than for the HER recipe (but the angle was bigger for the last two recipes).

4. Conclusion

In this paper we proved that using a variable isotropy process (based on mixing of isotropic and anisotropic etching process during the same etching run) it was possible to obtain tapered via holes with a good control over the wall angle-in this case angles obtained were between 14º and 18º. Also, after via manufacturing, it was possible to deposit a continuous seed layer which can be used for via filling by electroplating, improving the adhesion over the walls and having a barrier layer (chromium in this case).

Although the process needs to be optimized for each mask dimension and for each depth (due to the sensitivity of the etching rate with depth, decreasing sharply with depth mainly in small cavities), this technique provides an easier and reliable way to obtain tapered via's, with a very good control over the walls angles that can easily be adapted to any ICP type equipment.

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References

[1] A. POLYAKOV, T. GROB, R.A. HOVENKAMP, H.J. KETTELARIJ, I .EIDNER, M.A. DE SAMBER, M. BARTEK, J.N. BURGHARTZ, *Comparison of Via-Fabrication Techniques for Through-Wafer Electrical Interconnect Applications*, Electronic Components and Technology Conference, p. 1466, 2004.

[2] C.S. PREMACHANDRAN, R. NAGARAJAN, C. YU, B. XIOLIN, C.S. CHOONG, *A Novel Electrically Conductive Wafer Through Hole Filled Vias Interconnect For 3D MEMS Packaging*, Electronic Components and Technology Conference, p. 627, 2003.

[3] N. LIETAER, P. STORAS, L. BREIVIK, S. MOE, *Development of cost-effective high-density through-wafer interconnects for 3D Microsystems*, J. Micromech. Microeng., **16**, pp. S29–S34, 2006.

[4] S.N. Subbarao, *et all*, *Method for Fabricating Via Holes in a Semiconductor Wafer*, US Patent (4), 348,253, Sep.7, 1982.

[5] D. VASILACHE, S. COLPO, S. RONCHIN, F. GIACOMOZZI, B. MARGESIN, *V-shape through wafer via manufactured by drie variable isotropy process*, International Semiconductor Conference (CAS), Sinaia-Romania, p. 235, 2010.

[6] F. MARTY, L. ROUSSEAU, B. SAADANY, B. MERCIER, O. FRANÇAIS, Y. MITA, T. BOUROUINA, *Advanced etching of silicon based on deep reactive ion etching for silicon high aspect ratio microstructures and three-dimensional micro-and nanostructures*, Microelectronics Journal, **36**, p. 673, 2005.

[7] B.L.P. GASSEND, L.F. VELÁSQUEZ-GARCÍA, A.I. AKINWANDE, *Design and Fabrication of DRIE-Patterned Complex Needlelike Silicon Structures*", J. MEMS **19**, p. 589, 2010.

[8] B.L.P. GASSEND, L.F. VELÁSQUEZ-GARCÍA, A.I. AKINWANDE, *Design and Fabrication of DRIE-Patterned Complex Needlelike Silicon Structures*, J. MEMS **19**, p. 589. 2010.

[9] C.-L. DAI, F.-Y. XIAO, Y.-Z. JUANG, C.-F. CHIU, *An approach to fabricating microstructures that incorporate circuits using a post-CMOS process*, J. Micromech. Microeng., **15**, p. 98, 2005.

[10] M. SHIKIDA, N. INAGAKI, H. SASAKI, H. AMAKAWA, K. FUKUZAWA, K. SATO, *The mechanism of selective corrugation removal by KOH anisotropic wet etching*, J. Micromech. Microeng., 20, 015038, 2010.

[11] R. LI, Y. LAMY,W.F.A. BESLING, F. ROOZEBOOM, P.M. SARRO, *Continuous deep reactive ion etching of tapered via holes for three-dimensional integration*, J. Micromech. Microeng., **18**, 125023, 2008.