Low-Loss Distributed 2-bit RF MEMS Phase Shifter for 60GHz Applications

Cheikh NDIAYE[1], Arnaud POTHIER[1], Cyril GUINES[1], Pierre BLONDY[1]

[1]XLIM UMR 6172, Université de Limoges /CNRS, 123 avenue Albert Thomas, 87060 Limoges, France
E-mail: cheikh-tidiane.ndiaye@xlim.fr, arnaud.pothier@xlim.fr, pierre.blondy@xlim.fr

Abstract. This paper presents the design of a low loss 2-bit digital phase shifter using a high-impedance coplanar transmission line periodically loaded with miniature RF-MEMS switched capacitors. This phase shifter is designed to generate four phase states with an accuracy of better than 2° and should be integrated to allow electronic steering of patch antenna in SIP complete communication module operating at 54.5 GHz. This phase shifter is composed of the series association of 18 unit cells organized in 2 independent bits thanks to DC biasing though decoupling MIM capacitors. At 54.5 GHz the targeted reflection loss matching should be better than -12 dB with insertion loss of as low as 1.5 dB whatever the phase state generated.

1. Introduction

Since a couple of years, phase shifters appear to be key components in any communication module that requires antenna with scanning and beam forming capabilities.

Several technologies are today available to produce highly integrated and high performance phase shifters in the millimeter wave frequencies spectrum. Hence phase shifter design using semiconductor components technology like FET or PIN diode have been for a long time favored ensuring high integration level and very fast reconfiguration capabilities (1-100ns) [2]. But nevertheless this technology generally implies high insertion losses as well linearity and power consumption troubles [3-4].

Today, other candidates are under study to overcome these drawbacks, as ferroelectric capacitors [5-8] that still requires doing compromises between loss and tunability capabilities or also RF-MEMS components ensuring both low insertion loss and power consumption with monolithic integration capabilities [9] with sometime some limitation in term of switching speeds and power handling.

Today there are three main topologies that have been exploited to achieve phase shifter design based on RF MEMS component technology. The first is based on the phase shift induced by a reflection line design which usually requires couplers or circulators The second is based on switchable delay line topology whereas the third uses the principle of a slow wave transmission line periodically loaded with switches or MEMS switched capacitors well known as DMTL (Distributed MEMS Transmission Lines) on which the phase shift introduced when MEMS are activated is given by [1]:

$$\Delta\phi = \frac{360\, fsZ_0\sqrt{\varepsilon_{eff}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right)\frac{\deg\text{rees}}{\sec\text{tion}} \tag{1}$$

It is expressed in terms of:

- f the operating frequency in Hz
- s the spacing between the MEMS switches in m
- Z_0 the characteristic impedance of the line in Ω
- ε_{eff} the effective dielectric constant of the substrate.
- c is the speed of light in vacuum in m/s
- Z_{lu} and Z_{ld} the impedances of the loaded line corresponding to up and down states of MEMS switches respectively in Ω.

The aim of our study is to prototype high performance 2-bit phase shifters combining low losses and low power consumption, able to generate four phase states [0°, 65°, 130°, 195°] to ensure the targeted 20 degrees beam steering on the radiating pattern of a millimeter frequencies antenna based on a four patches array. The targeted frequency band is quite wide (52-57GHz) implying to achieve a broadband performance, that why DMTL phase shifter topology has been favored. This approach is also compatible with the final SIP (System in Package) integration expected in this work.

2. Operating Principle of a DMTL Phase Shifter

As illustrated in Fig. 1, one approach to design a DMTL phase shifter in millimeter frequency band is to use a high-impedance coplanar line periodically loaded by MEMS switched capacitors. Thus the phase shifter design consists in cascading identical unit cells that allows obtaining a phase shift proportional to the number of cells used. By appropriately sizing the MEMS components and their periodic spacing on the transmission line, we can lower the impedance of the transmission line from its unloaded value Z_0 to loaded impedance given by [10]:

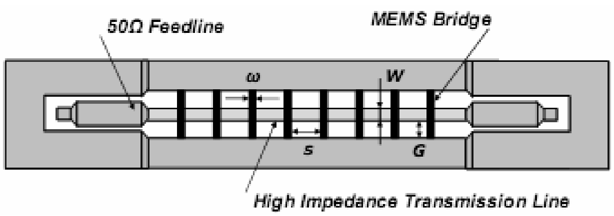


Fig. 1. Structure of the DMTL phase shifter from the top view.

$$Z_l = \sqrt{\frac{L_t}{C_t + C_b / s}} \quad (2)$$

where C_t and L_t are the per unit-length capacitance and inductance of the unloaded high-impedance transmission line and C_b (C_{bu} for the OFF state and ON state for C_{bd}) and s are the RF-MEMS switch capacitance and periodic spacing, respectively. In addition to changing the transmission-line impedance, phase velocity is also decreased due to the capacitive load and is given by [10]:

$$v_l = \sqrt{\frac{1}{L_t(C_t + C_b / s)}} \quad (3)$$

So the maximum expected return loss level RL_{max} can be set judiciously choosing the optimal impedance for loaded transmission line.

Thus the periodically loaded transmission line can operate over a wide frequency range from DC up to Bragg frequency of the device corresponding to a cutting frequency where the propagated wavelength begins to be very close to the RF-MEMS switches period spacing. This frequency can be easily computed using (6) and set the size of the phase shift elementary cell as function of the targeted bandwidth of operation of the phase shifter [11]:

$$f_{Bragg} = \frac{1}{\pi \cdot s\sqrt{L_t(C_t + C_b / s)}} \quad (4)$$

3. RF Design

A. Miniature MEMS switched capacitors

For the switched capacitors design that will load periodically the slow wave coplanar line used as phase shifter, we have opted for a miniature MEMS component topology whose dimensions are 5 to 10 times lower than conventional RF MEMS components. As shown in [12], this approach also allows to achieve switching times of less than one microsecond but also to be less sensitive to temperature changes and the effects of charge trapping at the root of many failures encountered in the conventional RF MEMS components. As illustrated in Fig. 2, these MEMS two states capacitors are based on a 60×30µm^2 gold movable membrane 350 nm thick and suspended 1µm above the lower capacitor RF electrode also used as biasing electrode. This electrode is covered with an insulating AlN film 200 nm thick. According to finite element electromechanical simulations performed using ANSOFT ANSYS, with this design these switches should require actuation voltages from 20 up to 30V and can generate a change in capacitance from 15fF to 90fF once actuated.

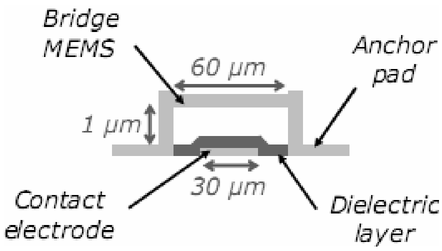


Fig. 2. Miniature RF-MEMS switched capacitor cross-view section.

B.2 bits DMTL phase shifter design

As shown in Fig. 3, each MEMS switched capacitor (C_{bu}, C_{bd}) is associated in series with a MAM capacitor C_s (Metal Air Metal) in order to avoid RF MEMS capacitance value dispersion in their down state. Indeed, the specificity of the MAM capacitor is to be mechanically unmoving allowing to ensure a fixed capacitance value.

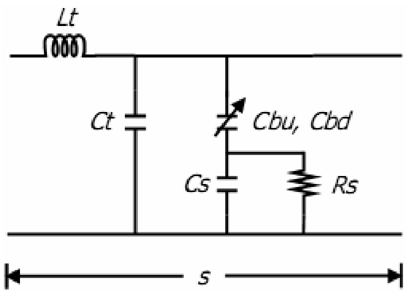


Fig. 3. Unit cell equivalent circuit model with the MEMS bridge.

Thus the load capacitance seen by the line is the series combination of the MEMS bridge capacitance C_b and the total lumped capacitance C_s (45fF) and is:

$$C_l = C_s C_b / (C_b + C_s) \quad (5)$$

when the MEMS bridge is in the up-state position, the bridge capacitance C_{bu} (15fF) is, in the limit, much smaller than C_s (45fF) and the effective capacitance seen by the transmission line, is C_{lu}≈C_{bu}. When a bias is applied on the line and the MEMS bridge is in the down-state position, the bridge capacitance C_{bd} (expected to be at least higher than 90fF) increases by a factor of 6 and becomes much larger than C_s (45fF)) thereby resulting in a load capacitance of C_{ld}≈C_s. The distributed capacitance can therefore be discretely controlled by the independent choice of C_{bu} and C_s. Our unit cell is designed to achieve 11 degrees phase shift at 54.5 GHz. Thus as shown in Fig. 4, by cascading 6 unit cells, a 65° degrees phase shift section is obtained whereas using 12 cells a 130 degrees phase shift can be achieved. For each of these group of cells, activation of MEMS switched capacitors will collectively and synchronous and independently from each other through the integration of DC decoupling MIM capacitors (300 fF) between the two bits. It allows generating the intermediate phase states (*i.e.* 65° and 130°). As illustrated in Fig. 4, the MEMS biasing is ensured by separate commands related to the central conductor of the waveguide through high impedance integrated resistor R_s (50-100kΩ). These resistances allow us to prevent any leakage of the RF signal into the bias network and maintain a low loss performance phase shifter.

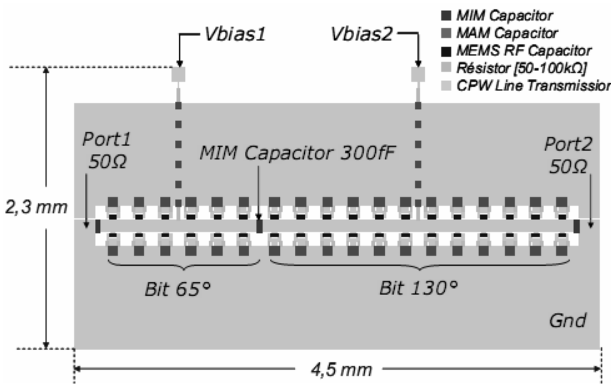
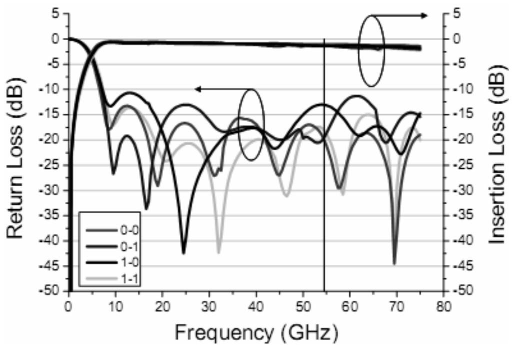


Fig. 4. Layout of the DMTL 2-bit phase shifter.

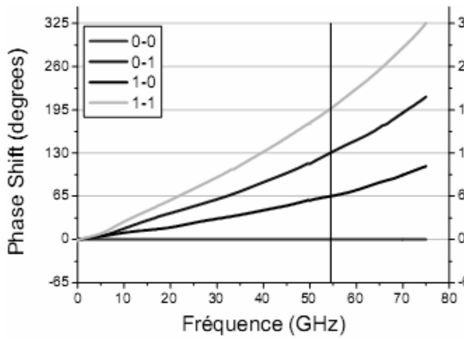
4. Conclusions

This paper illustrates the potential of miniature RF-MEMS switched capacitors to design low-loss digital type distributed RF-MEMS phase shifters in millimeter frequencies. The electromagnetic simulations performed on this design using the software 2.5 D Momentum confirmed that the number of cells retained will achieve the desired level of total phase shift with a phase error acceptable. Also as shown in Fig. 5-(a) and 5-(b), the matching level remains well below -12 dB in the frequency range covered (52-57 GHz), while the total loss level is estimated better than 1.5 dB regardless the phase state looked for. Thus, at 54.5 GHz, as well Table 1 summarizes simulations results that seem very promising. The first phase-shifters fabrication is still on-going in our laboratory

(Fig. 6). Unfortunately, on the first fabrication run the biasing resistances were not working properly due to fabrication process troubles. This problem will be normally fixed quickly. First RF measurements (Fig. 7) are still in good agreement with expected performances, but since bit cannot be activated for instance, only one state has been successfully measured. A second fabrication run is running, last results with operating MEMS capacitors are expected in the following weeks and will be presented during the MEMSWAVE conference this year.



a)



b)

Fig. 5. Simulation results of the 2-bit DMTL phase shifter.
(a) Return Loss and Insertion Loss, (b) Phase Shft.

Table 1. Expected Performance of th 2-Bit MEMS Phase Shifter at 54.5 GHz

Binary combination	0-0	1-0	0-1	1-1
Desired phase shift	0,0°	65,0°	130,0°	195,0°
Simulated phase shift	0,0°	65,4°	129,4°	193,8°
Phase error	0,0°	0,4°	0,6°	1,2°
Return loss (dB)	-20	-13	-19,5	-18
Insertion loss (dB)	-0.8	-1,2	-1,1	-1,2

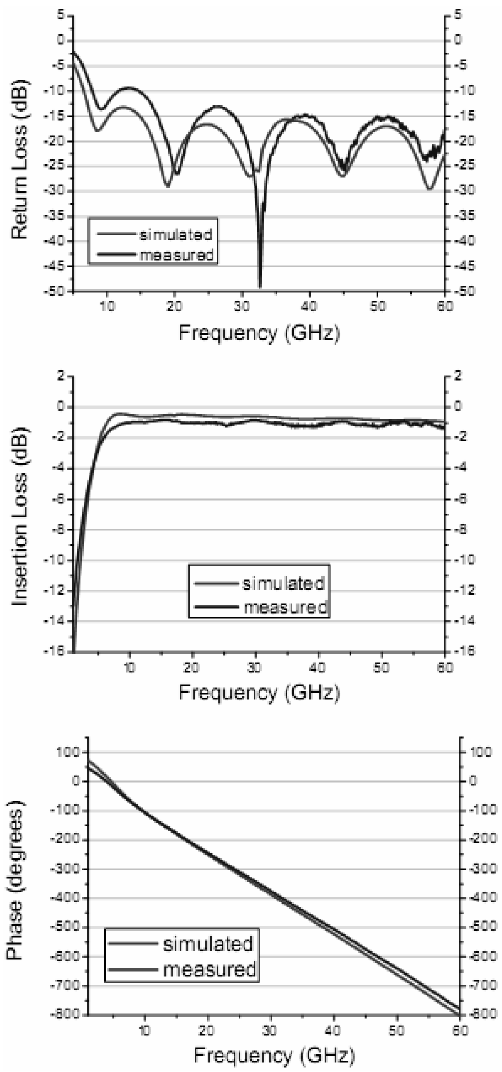


Fig. 7. RF performance of phase shifter in their 0-0 state.

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