# Multilayer Micromachining Technology for the Fabrication of Ka Band Filters

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**Abstract.** This paper presents the manufacturing and testing of a new type of compact and low loss 4th order Ka band filter in multilayer micromachining technology. The filter is based on λ/2 TEM Si membrane resonators placed inside shielding cavities and short-circuited at both anchored ends. The membranes and the cavities are realized by DRIE on SOI wafers and are metalized by gold electroplating. The filter is realized by stacking and bonding six silicon layers for a reduced footprint and area occupation. The RF measurements are very promising, showing insertion loss better than 3dB and Q factors above 500 in Ka-band. Shear tests demonstrated good adhesion of bonded layers and preliminary thermal and mechanical shock test indicated the filter robustness.

## 1. Introduction

Micromachining technology is one of the most promising alternatives for the realization of high RF performance, low-mass and compact Ka-band filters required for on-board satellite telecommunication [1, 2]. Such a technology allows the realization of metallized cavities and suspended membranes in Silicon or SOI (Silicon On Insulator) substrates. A reduction of device footprint can be obtained with a multilayer approach stacking several cavities by bonding techniques [3, 4].

By properly designing both the input and output planar ports on the same layer it is possible to obtain surface mountable devices that can be easily integrated in standard printed circuits [5].

This paper presents the fabrication technology developed to realize a new type of narrow band 4th order Ka band filter based on the combination of multilayer and micromachining technologies. The filter consists of four resonators placed on

two different levels to reduce the area occupation. Each element is based on a λ/2 TEM membrane resonator suspended inside a shielding cavity and short-circuited to the cavity walls. [6].

The cavities are realized by bonding together two micromachined silicon layers obtained by *Deep Reactive Ion Etching* (DRIE) of SOI wafers. The first one realizes the upper cavity while the second one comprises the 20μm thick silicon membrane and the bottom half of the cavity. All membrane and inner cavity surfaces are metalized by electroplated gold.

The cavities are placed on two levels as schematically reported on Fig 1. Cavities 1–2 as well as cavities 3–4 are coupled vertically while cavities 2–3 and 1–4 are coupled horizontally. A top layer is used as a lid for cavities 1 and 4 and for input and output by depositing on the upper surface microstrip feeding lines that are coupled in resonant mode to the cavities by a thin slot opened in the common ground plane. *Through silicon via's* (TSV) are required for front to back ground connections. The filter design is presented in [7].

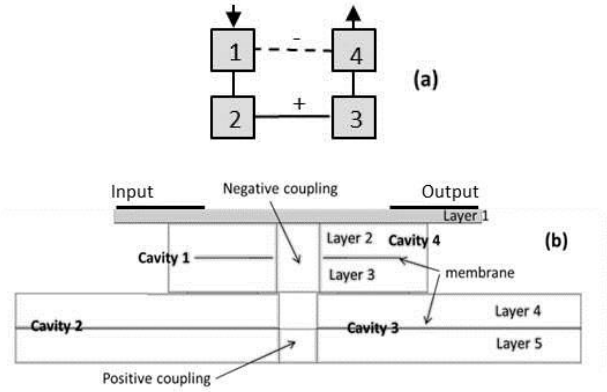


**Fig. 1.** 4th order Ka band filter topology (a) and schematic cross section (b).

The complete filters are fabricated by stacking six silicon layers: a base layer, four intermediate layers (two layers for each membrane resonator and shielding cavity) and a top layer that provides the RF input and output. A schematic cross section showing the different layers is reported in Fig. 2. The layers are stacked and assembled by gold to gold thermo-compressive bonding, the bonding area is defined by sealing rings realized on the die edges.

Single resonator test structures and two versions of the filter were realized considering surface mounting as well as microstrip to CPW transition to test the devices using probes.

## 2. Fabrication Process

For the fabrication of the different layers two processes are required: a 6 masks process for the top plate and a 3 mask process for the intermediate layers. The bottom blank layer is obtained by gold plating an oxidized silicon wafer.

In order to reduce the development costs in the first run the chips for intermediate layers were all realized on the same wafer and after dicing the corresponding dies were stacked and assembled by thermo-compression using a flip chip bonder.

The top layer is fabricated on 275 µm thick <100> p type double side polished 5000 Ωcm high resistivity silicon wafers. The fabrication process starts with photolithography and plasma etching to define on the wafer backside the 2 µm thick 50 µm wide sealing rings which define the area for layer to layer bonding at the edge of each device (Fig 3a).

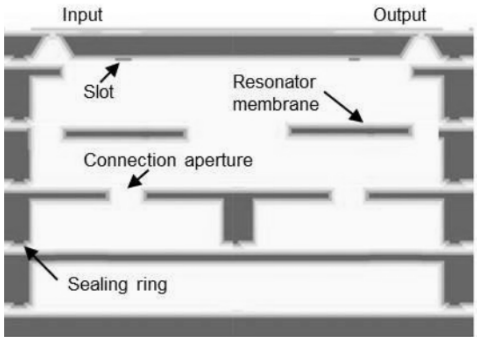


**Fig. 2**. Schematic cross section of a filter showing the 6 layers.

To realize the hard mask layer on both sides 1 µm thick oxide is grown by steam oxidation at 975°C followed by the deposition of 150 nm thick silicon nitride by LPCVD at 775°C and 300 nm oxide from TEOS at 718°C. The mask for the bottom via's is printed and the dielectric layer dry etched on the wafer backside (Fig 3b). The through silicon via's (TSV), necessary for the front to back ground connection, are obtained by removing the silicon substrate by anisotropic wet etching using *Tetra-Methyl-Ammonium-Hydroxide* (TMAH) to achieve 54.7° angled walls (Fig 3c). The fabrication proceeds by removing selectively the hard-mask layer from the backside of the wafer with a dry etching process to bare silicon leaving the front side exposed membranes nearly untouched because the efficiency of the etching is very low in the narrow holes (less than 50 x 50 $\mu m^2$). The exposed silicon surface is steam oxidized to obtain a 1 µm thick oxide to passivate the wafer backside and the TSV walls (Fig 3d). In the next step the TEOS oxide on top of the wafer front side is removed by dry etching and then the silicon nitride is etched by hot phosphoric acid living on the front side only

1μm thermal oxide. The backside of the wafer is coated with a Cr/Au seed layer by PVD and the slots through which the RF signals enters and exit from the cavity are defined. A negative dry film is used because the lamination of the dry film is almost unaffected by the via's holes. The seed layer is wet etched inside the slots and after resist removal a 2.5μm thick gold layer was electro-plated from a cyanide based gold bath to complete the backside processing (Fig 3e).

To provide the electrical connection to the bottom gold layer the top via holes are defined by lithography and the front side oxide membrane dry etched (Fig 3f). A Cr/Au seed layer is deposited on top of the wafers, patterned to define the microstrip input and output RF lines and a 2,5 μm thick gold layer is selectively electroplated. After resist removal the seed layer is wet etched and the gold is annealed at 190 °C for 30 min to improve the adhesion (Fig 3g). To complete the fabrication process the front- side of the wafers is coated with 100 nm thick PECVD oxide layer and the contact holes for the pads are defined and wet etched with buffered oxide etcher (Fig 3h).

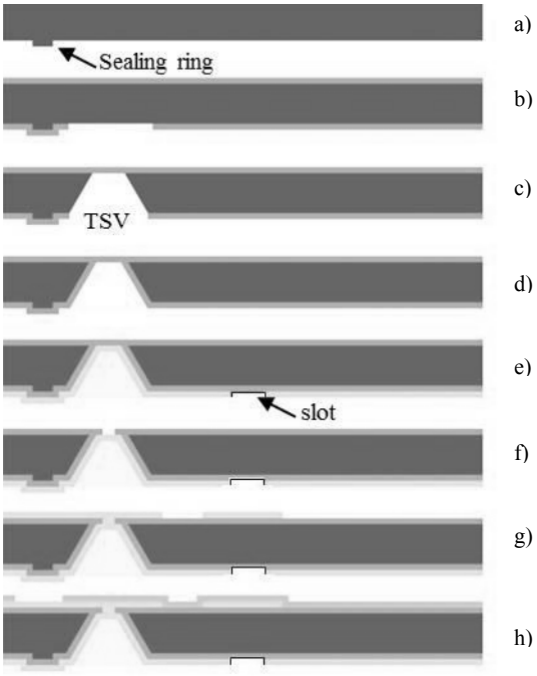


**Fig. 3.** Processing sequence for the top layer of the Ka band filter.

To fabricate the membranes and the cavities of the intermediate layers DRIE is used to obtain almost vertical sidewalls. The DRIE process is sensitive to the

exposed area and the depth of etching changes from structure to structure and from wafer border to wafer centre. To overcome this potential problem SOI wafers have been chosen as substrate material because the oxide layer between the handle wafer and the top layer can be used as an effective etch-stop for the etch process, allowing an easy and precise control of the membrane thickness within the tolerances of the SOI top layer, typically +/-0.5 μm.

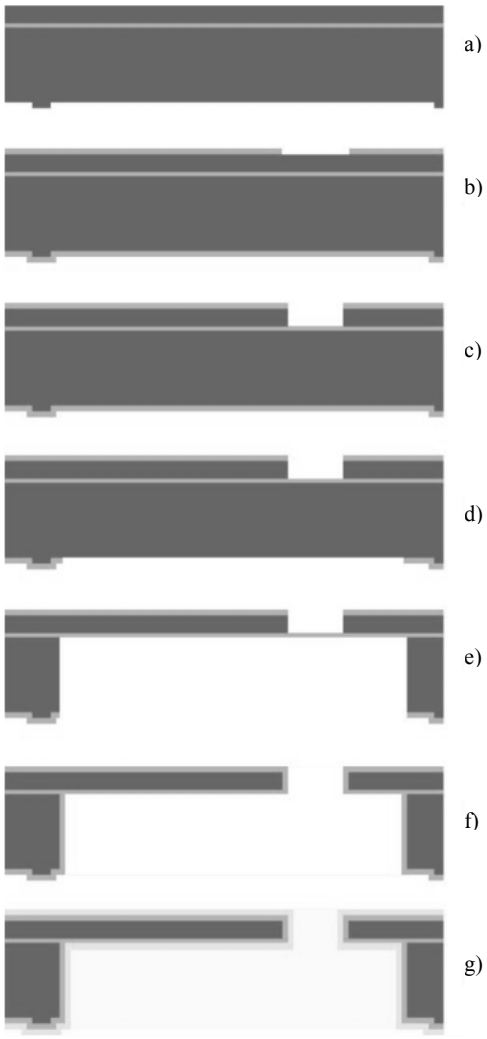


**Fig. 4.** Processing sequence for the middle layers of the Ka band filter.

The substrates for the intermediate layers process are low resistivity double side polished SOI wafers with a 625 μm thick CZ <100> p type handle wafers, a 1 μm thick buried oxide layer and a 20 μm thick CZ <100> p type device layer. After defining and dry etching the sealing rings on the wafer backside (Fig 4a), a 300 nm thick thermal oxide is grown on both sides by steam oxidation at 975°C. The etch windows for membrane resonators and connection apertures are defined on the wafer front side and the oxide mask dry etched (Fig 4b).

A short DRIE process is used to remove the 20 μm device layer of the SOI up to the buried oxide layer, which acts as an etch stop, and the resist is removed by oxygen plasma (Fig 4c).

A 500 nm thick layer of pure aluminum is deposited by sputtering on the wafer backsides. Next the hard mask for the etching of the bottom cavities is defined by photolithography with thick resist and the aluminum layer and the underneath oxide layer are removed by dry etching (Fig 4d). The cavities are then etched from the backside with a DRIE process for the full depth of the handle wafer by using the buried oxide as an etch stop. (Fig 4e). The residual resist and the passivation polymers on the cavity sidewalls were removed by oxygen plasma and the aluminum layer of the hard mask is removed by wet etching.

After applying an oxygen plasma on both sides, to remove any organic contaminant, the components were stacked starting from the blank bottom plate and adding successively the intermediate layers and the top plate. Each layer was aligned on the previous one with an accuracy in the order of 10 μm and preassembled applying a load of 2 kg (corresponding to a pressure of about 10 MPa) for a few minutes. Once all elements have been stacked correctly the full stack was loaded with 2 kg and heated at 350°C for 45 min by using an interposer plate with the same footprint of the device to apply a uniform pressure on the sealing rings.

The back and front side oxide layers are removed till the bare silicon by dry etching using a high uniformity recipe. Dry etching was chosen in order to avoid the formation of a notch at the level of the buried oxide which would impair the electrical continuity between front and backside of the wafer. After this, a 1 μm thick insulating thermal oxide is grown uniformly on all bare silicon surfaces (Fig 4f) and the wafers are coated with a gold seed layer on both sides. To increase the step coverage on the vertical sidewalls of the cavities, the wafers were mounted at an angle of about 30° with respect to the normal position and two gold deposition were done rotating the wafers of 180° after the first one. To have a uniform metallization a 2.5 μm thick gold film was grown on both sides by electroplating in a fountain plater (Fig 4g). At the end the wafers were annealed at 190°C for 30 min in order to sinter the gold layers.

The wafers were diced by a diamond blade paying attention to not damage the fragile membranes with the water jet of the dicing saw. The dies

corresponding to different layers were selected and assembled by thermo-compression using a flip-chip bond aligner model TRESKY T-3000-FC3.

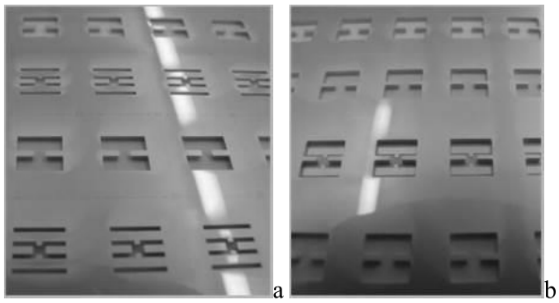


**Fig. 5.** Presents details of a processed wafer showing some of the intermediate layers dies.

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**Fig. 6.** Pictures of fabricated 4th pole filters.

### 3. Experimental Results

A few wafers of each kind were processed and diced. Each die was optically inspected and any defective component was discarded. On the top layer a few via's were not completely open while on the intermediate layer a few membranes

were broken during dicing and handling. The majority of the dies were good and about 80 filters could be assembled (Fig 6).

At the end of the fabrication the suspended membrane were almost flat, a slight deflection of just a few micron (2–4) was measured by optical profiler (Fig.7).

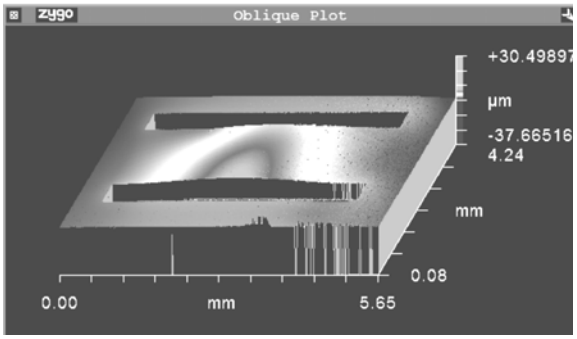


**Fig. 7.** Optical profiler measurement of a resonator membrane showing a slight deflection of a few microns.

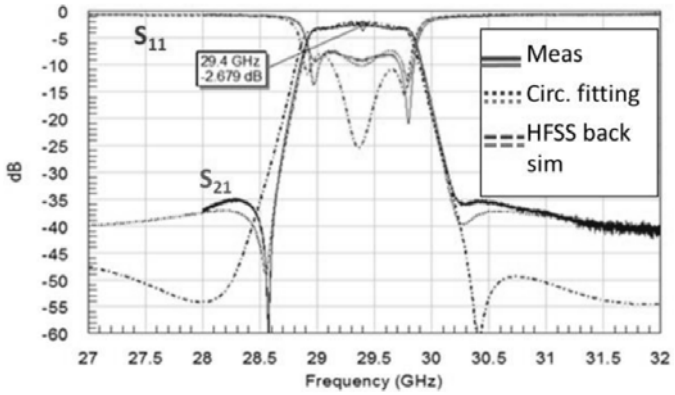


**Fig. 8.** RF measurements compared with circuital (AWR) and HFSS back simulation, accounting for the actual cavity dimensions.

The filter cavities resulted wider than designed due to not optimal setting of the etching parameters. To reduce nanograss formation, *i.e*. a very rough bottom surface consisting of silicon nanopillars created by the micro- masking effect of polymer residues, the oxygen flow was increased. This reduced the effectiveness of the BOSCH process [8] increasing the removal of protective polymers from the sidewalls and the lateral overetching was much higher than expect, about 60 – 80µm.

Moreover the residual roughness of the bottom surface induced a rough electroplated gold surface.

Figure 8 shows the measured S-parameters of manufactured filter in comparison with circuital and back simulations taking in account the real (measured) cavity dimensions. Due to the longer membranes and larger coupling windows between cavities the resonant frequency down shifted of about 900 MHz respect to the nominal 30 GHz and the return loss was worse than expected. This can be solved in the next fabrication run either by a DRIE process optimization or a cavity mask under sizing.

The filter shows insertion loss below 3dB and a Q factor above 500, slightly lower than predicted very likely due to the high roughness of the cavity bottom interface.

To check the bonding strength shear tests were performed on test samples, which showed that a force of about 4 kg was required to detach the bonded layers indicating good adhesion.

Environmental tests are on-going to demonstrate the space compatibility of the filter. Preliminary tests didn't reveal failures or S-parameters modifications on samples after 10 thermal shock cycles from – 30 °C to 100 °C and after mechanical shocks.

## 4. Conclusion

A new type of compact and low loss 4th order Ka-band filter was fabricated using a combination of multilayer and micromachining technology.

$\lambda/2$ TEM resonators were realized by metalized silicon membranes placed inside shielding cavities and the cavities are placed on two levels to reduce the footprint.

Through silicon via's on the top level were realized by TMAH anisotropic etching while membranes and cavities were realized by DRIE on SOI wafers and metalized by gold electroplating. The filters were obtained by stacking and gold to gold thermo-compression bonding six silicon layers.

The RF measurements showed insertion loss better than 3dB and Q factors above 500 in Ka-band. The resonant frequency presented a down shift respect to the nominal value due to etching non-idealities that can be solved in the next fabrication run.

Shear tests demonstrated good adhesion of the bonded layers and preliminary thermal and mechanical shock tests indicated the filter robustness.

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## References

[1] L. HARLE, L. KATEHI, *A Silicon Micromachined Four-Pole, Linear Phase Filter*, IEEE Trans. on Microwave Theory and Techniques, **52**(6), 2004.

[2] Y. WANG, M. KE, M.J. LANCASTER, *Micromachined 38 GHz cavity resonator and filter with rectangular-coaxial feed- lines*, IET Microw. Antennas Propag., **3**, pp. 125–129, 2009.

[3] L. HARLE, L. KATEHI, *A vertically integrated Micromachined Filter*, IEEE Trans. on Microwave Theory and Techniques, **50**(9), 2002.

[4] M. STICKEL, P. KREMER, G. V. ELEFTHERIADES, *A Millimeter- Wave Bandpass Waveguide Filter Using a Width-Stacked Silicon Bulk Micromachining Approach*, IEEE Microwave and Wireless Components Letters, **16**(4), 2006.

[5] SANGSUB SONG, CHAN-SEI YOO, KWANG-SEOK SEO, *W- Band Bandpass Filter Using Micromachined Air-Cavity Resonator With Current Probes*, Microwave and Wireless Components Letters, IEEE, **20(**4), pp. 205–207, April 2010.

[6] L. PELLICCIA, P. FARINELLI, R. SORRENTINO, *Micromachined Filters In Multilayer Technology For On-board Communication Systems in Ka-band*, 2013 IEEE MTT-S International Microwave Symposium Digest (IMS), Seattle, 2-7 June 2013.

[7] P. FARINELLI, L. PELLICCIA, BENNO MARGESIN, R. SORRENTINO, *Ka-band Surface-Mountable Pseudo-elliptic Filter in Multilayer Micromachined Technology for On-board Communication Systems*, 2016 IEEE MTT-S International Microwave Symposium Digest (IMS 2016), San Francisco USA, 22-27 May 2016.

[8] S.A. McAULEY, H ASHRAF, L ATABO, A CHAMBERS, S HALL, J HOPKINS and G NICHOLLS, *Silicon micromachining using a high-density plasma source*, J. Phys. D: Appl. Phys. **34**, pp. 2769–74, 2001.