NOVEL TECHNOLOGIES FOR MICROWAVE AND MILLIMETER WAVE DEVICES AND CIRCUITS

NOI TEHNOLOGII PENTRU
DISPOZITIVE ŞI CIRCUITE DE MICROUNDE
ŞI UNDE MILIMETRICE

NOVEL TECHNOLOGIES FOR MICROWAVE AND MILLIMETER WAVE DEVICES AND CIRCUITS

EDITOR:

Alexandru Müller

EDITURA ACADEMIEI ROMÂNE

Bucureşti, 2017

Copyright © Editura Academiei Române, 2017.
All rights reserved.

The responsibility for originality and the contents of the articles lie exclusively with the authors.

Address: EDITURA ACADEMIEI ROMÂNE
Calea 13 Septembrie nr. 13, sector 5,
050 711, Bucureşti, România,
Tel. 4021-3188146, 4021-3188106
Fax: 4021-3182444
E-mail: edacad@ear.ro
Internet: http://www.ear.ro

Peer reviewers: Acad. Dan Dascalu, Prof. Gheorghe Brezeanu

Descrierea CIP a Bibliotecii Naţionale a României

Novel technologies for microwave and millimeter wave devices and circuits / ed.: Alexandru Muller

- Bucureşti : Editura Academiei Române, 2017
ISBN 978-973-27-2809-3

I. Muller, Alexandru (ed.)

62

Editorial assistant: Mihaela Marian
Computer operator: Anişoara Marinescu
Cover: Elena Stanila, Anişoara Marinescu

Passed for press: Size: 16 / 70 × 100.
Printed sheets:
D.L.C. for large libraries: 621.38.029.6
621.37.029.6
D.L.C. for small libraries: 62

CONTENT

FOREWORD

The MEMSWAVE conference (originally a workshop) has been taking place every year since 1999. The event was generated by the FP4 European Project MEMSWAVE – Micromachined Circuits for Microwave and Millimeter Wave Applications (1998 – 2001) coordinated by Alexandru Müller (IMT Bucharest). It was the first IST project coordinated by a team from an Eastern European country. The project was nominated between the ten finalists (from 108 projects), for the Descartes Prize Competition of the EC, in 2002.

The first edition was held in Sinaia (Romania) in 1999, as an within the MEMSWAVE project, but open to the participation from outside the consortium. It was idea of Dan Dascalu (by that time CEO of IMT Bucharest). It was followed by the similar events in Budapest (2000) and in Sinaia again, (2001), when Robert Plana (at LAAS – CNRS Toulouse at that time) proposed to transform it in an itinerant European event. In 2016, after 15 years MEMSWAVE have returned to Romania with its 17th edition.

The main papers of the 2001 Sinaia edition have been published in a special volume of the series Micro and Nanoengineering namely *Micromachined Microwave Devices and Circuits* The Publishing House of the Romanian Academy.

The present volume contains the selected papers presented at the 17th edition of the MEMSWAVE conference organized by IMT Bucharest in July 2016 at its' headquarters, in Bucharest.

This volume containes original papers presenting recent collaborative research in novel technologies for microwave and millimeter wave devices and circuits, research performed in universities, companies and research centers. The authors are from IMT Bucharest, LAAS Toulouse, FORTH Heraklion, FBK-irst Trento, RF Microtech, Athens University, IHP Frauenhofer Inst., Rohde & Schwarz GmbH, Silicon Radar GmbH, Institute of Electron Devices and Circuits, Ulm University, KTH Royal Institute of Technology, Stockholm, Sensor Systems Department, Acreo Swedish ICT.

The volume addresses a wide RF MEMS topic. Some papers present MEMS membrane composite membrane layer system for MEMS varactor, flexible Kapton technology for V-band applications, the electrical properties of silicon nitride dielectric films with embedded Multi-Walled Carbon Nanotubes, that can be used in RF MEMS capacitive switches, the manufacturing and testing of a new type of compact and low loss 4th order Ka-band filter in multilayer micromachining technology.

One paper presents first ever RF MEMS switch reported to be operating above 220 GHz. It is a 500-750 GHz waveguide based *Single-Pole Single-Throw*

(SPST) switch achieving a 40% bandwidth. Other papers address the analysis of pull-up capacitance-voltage characteristic of MEMS capacitive switches by introducing an analytical model that takes into account the case of a real device, where the charge is not uniformly distributed at the surface of the dielectric film and the switch armatures are not parallel and on-chip high-voltage charge pump integrated in a 0.13 µm SiGe:BiCMOS technology intended to be used for the actuation of BiCMOS embedded RF-MEMS devices like switches and varactors.

The Editor

September 2017

Micromachined Waveguide Integrated RF MEMS Switch Operating between 500-750 GHz

U. SHAH[1], T. RECK[2], E. DECROSSAS[2], C. JUNG-KUBIAK[2], H. FRID[1], G. CHATTOPADHYAY[2], I. MEHDI[2], and J. OBERHAMMER[1]

[1]KTH Royal Institute of Technology, Stockholm, Sweden
[2]Jet Propulsion Laboratory, Pasadena, CA, 91109 USA

Abstract. This paper presents a 500-750 GHz waveguide based single-pole single-throw (SPST) switch achieving a 40% bandwidth. It is the first ever RF MEMS switch reported to be operating above 220 GHz. The switch is based on a MEMS-reconfigurable surface which can block the wave propagation in the waveguide by short-circuiting the electrical field lines of the TE10 mode. The switch is designed for optimized isolation in the blocking state and for optimized insertion loss in the non-blocking state. The measurement results of the first prototypes show better than 15 dB isolation in the blocking state and better than 3 dB insertion loss in the non-blocking state for 500-750 GHz. The higher insertion loss is mainly attributed to the insufficient metal thickness and surface roughness on the waveguide sidewalls. Two switch designs with different number of blocking elements are fabricated and compared. The overall switch bandwidth is limited by the waveguide only and not by the switch technology itself.

Index Terms. Micromachined waveguide, RF MEMS, waveguide switch, switch, submillimeter-wave, terahertz, THz.

1. Introduction

The submillimeter-wave frequency band has an increasing scientific and industrial interest because of its applications in spectroscopy, radar, imaging systems, radio astronomy, material characterization, and ultra-high bandwidth wireless data communication. The unavailability of commercial components at these frequencies [1] creates the terahertz gap which presents an opportunity for devices based on Microelectromechanical systems (MEMS). MEMS devices are ideal for submillimeter-wave applications because of their low loss, low power consumption, high linearity and large bandwidth. MEMS based waveguide switches can replace the conventional rotary motor-based mechanical switches

which are bulky, heavy, requires high power and have a very slow response time. MEMS waveguide switches using electrostatic actuators have already been implemented [2] and more recently the actuators have been integrated inside the waveguide channel [3]. Moreover, MEMS based waveguide switches have been shown to perform well up to a frequency of 110 GHz [4]. MEMS-based RF devices are rare above 110 GHz and so far only two devices: a switchable stub [5] and a phase shifter [6] have been reported by the authors functioning up to a maximum frequency of 600 GHz. In addition, micromachined waveguides have shown promising results even up to 2.7 THz [7].

In this paper, we report on a fully functional RF MEMS waveguide switch based on a MEMS-reconfigurable surface operating at the center frequency of 625 GHz and with a bandwidth of 40 % in the frequency band between 500-750 GHz. It is the first ever RF MEMS switch operating above 220 GHz. The bandwidth of the switch is limited only by the waveguide and not by the switch technology itself.

2. Concept and Design

The single-pole single-throw (SPST) switch concept is shown in Fig. 1 and it is based on a MEMS reconfigurable surface inserted perpendicular to the wave propagation. The MEMS reconfigurable surface can short-circuit the electrical field lines in the TE_{10} mode thus blocking the wave propagation. It consists of vertical columns forming the contact cantilevers which are connected to horizontal bars. The contact cantilevers are grouped into a set of fixed and a set of movable cantilevers. The fixed set is anchored and the movable set is mechanically connected to electrostatic comb drive MEMS actuators via the horizontal bars. The

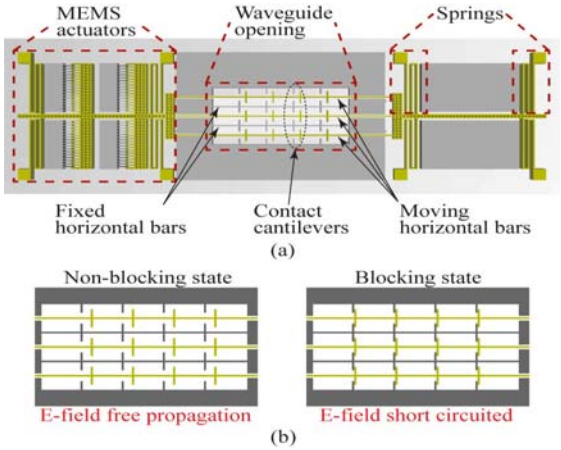


Fig.1. MEMS waveguide switch concept: (a) schematic cross-section of the switch, and (b) Non-blocking and blocking state of the switch.

comb-drives are placed to one side of narrow walls of the waveguide. In the non-blocking state (Fig. 1b), the vertical columns are not in contact and thus allow the electromagnetic wave to propagate freely through the MEMS reconfigurable surface. In the blocking state (Fig. 1b), the movable vertical columns are laterally displaced by the electrostatic actuators and brought into contact with the fixed vertical columns. This forms closed vertical columns in the path of the wave propagation, therefore blocking the electromagnetic wave propagation through the MEMS reconfigurable surface by short-circuiting the electric field lines of the dominant TE_{10} mode.

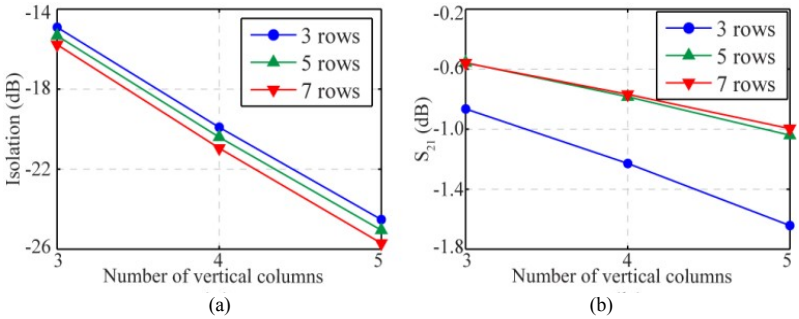


Fig. 2. Design parameter study at 625 GHz to evaluate the influence of the number of vertical columns and horizontal bars: (a) Isolation in the blocking state, and (b) S21 in the non blocking state.

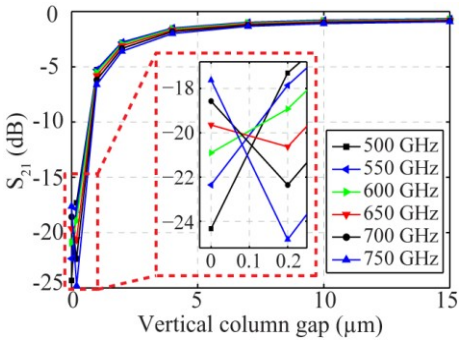


Fig. 3. (Color on line). Design parameter study to evaluate the influence of the vertical column gap on S21, simulated for the lossless case of the nominal design (5 horizontal bars and 4 vertical columns).

The number of vertical columns and horizontal bars has a strong influence on the ability of the MEMS reconfigurable surface to block or unblock the wave propagation. This number is optimized using full-wave simulations to achieve a

low loss transmission through the reconfigurable surface when in the non-blocking state and to achieve a high isolation when in the blocking state. Increasing the number of vertical columns improves the isolation in the blocking state but increases the insertion loss in the non-blocking state. The horizontal bars are perpendicular to the electric field lines in the waveguide and therefore do not impact the performance significantly in non-blocking state. Fig. 2 shows the design optimization simulations carried out at 625 GHz to select the best combination of horizontal bars and vertical columns for the waveguide switch. The design with 5 horizontal bars and 4 vertical columns achieves the best performance where the insertion loss in the non-blocking state is below 0.8 dB and the isolation in the blocking state is below 20 dB. Fig. 3 shows the simulated S_{21} of the nominal design (5 horizontal bars and 4 vertical columns) for different vertical column gaps. There is no significant improvement in the insertion loss for the nonblocking state when the vertical column gap is above 10 μm. A 15 μm gap is selected in the non-blocking state for the designs. Isolation of 20 dB is achieved for a vertical column gap of 200 nm in the blocking state. This gap is used in the simulations to better model the actual contact between the vertical columns. This is needed to compensate for variations in the etch profile and surface roughness of the fabricated designs.

The width of each vertical column is 4 μm with an overlap of 8 μm in the non-blocking state. The rectangular waveguide design has standard WR-1.5 dimensions 380 μm × 190 μm.

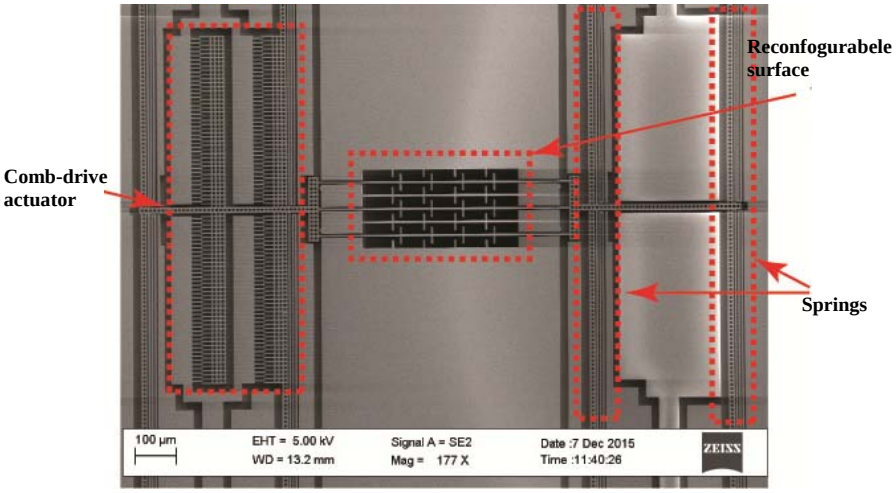


Fig. 4. SEM image of a fabricated prototype device.

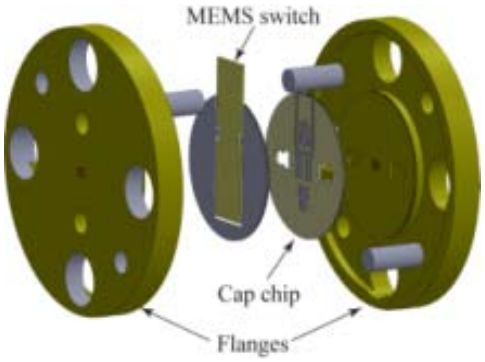


Fig. 5. Exploded 3-D view of mounting/assembly of the MEMS waveguide switch into standard WR-1.5 waveguide.

3. Fabrication and Assembly

The MEMS waveguide switch is fabricated in a two mask SOI RF MEMS micromachining process. The waveguide opening is made by doing the DRIE of the handle wafer (400 μm). This is followed by DRIE of the device layer (30 μm) to make the MEMS reconfigurable surface. The moving structures are free etched by wet etching of the buried oxide layer (3 μm) using hydrofluoric acid which is followed by a critical point drying step. A 900 nm thick gold layer is sputtered on the handle wafer and a 200 nm thick gold layer is sputtered on the device layer. The total chip size including contact pads and bias-line is 3.07 mm × 10.58 mm. Fig. 4 shows an SEM image of a fabricated device.

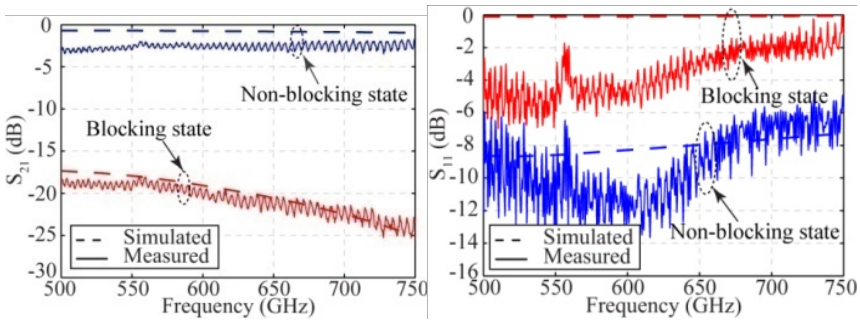


Fig. 6. (Color on line). Measured and simulated normalized S-parameters of the fabricated MEMS waveguide switch (5 horizontal bars and 4 vertical columns) in the two actuation states.

Fig. 5 shows an exploded 3-D schematic drawing, illustrating how the MEMS switch chip is mounted between two waveguide flanges. The MEMS switch chip is aligned to the flanges using omega-shaped alignment structures [8].

4. Measurements

Fig. 6 shows the measured and simulated insertion and return loss of the switch with 5 horizontal bars and 4 vertical columns. The measurements are normalized to a reference measurement done without the MEMS waveguide switch to remove the loss of the measurement fixture. The switch behaves exceptionally broadband over the whole design frequency range of 500-750 GHz with the isolation better than 15 dB in the blocking state. The insertion loss in the nonblocking state is 2 dB higher when compared to the lossless simulation. This is due to the combination of the insufficient gold thickness and surface roughness on the waveguide sidewalls of the MEMS switch. This was confirmed by comparing the insertion losses of two waveguide switches with different gold thicknesses. The measured and simulated return loss shows relatively good agreement except for the higher losses. Fig. 7 shows the measured isolation as the actuation voltage is ramped. The gap between the vertical columns is reduced by increasing the actuation voltage up to 40 V. Increasing the actuation voltage above 40 V no longer influences the isolation implying that the vertical columns make contact at 40 V.

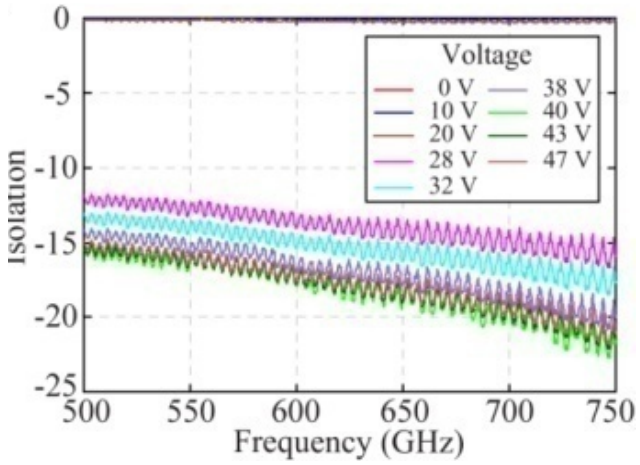


Fig. 7. (Color on line). Measured isolation as a function of applied voltage.

Fig. 8 shows the measured normalized S-parameters of the switch with 5 horizontal bars and 3 vertical columns. Reducing the number of vertical columns from 4 to 3 reduces the isolation in the blocking state from 15 dB (Fig. 6) to 12 dB

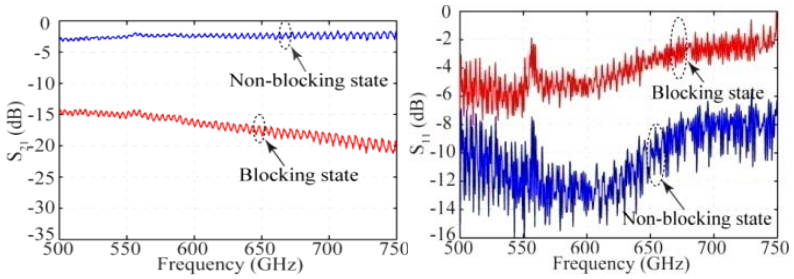


Fig. 8. (Color on line). Measured normalized S-parameters of the fabricated MEMS waveguide switch (5 horizontal bars and 3 vertical columns) in the two actuation states.

at 500 GHz. However, no improvement in the insertion loss in the non-blocking state is observed since the losses are dominated by the waveguide loss in the switch.

5. Conclusion

This paper reported on the design, fabrication and evaluation of the first ever submillimeter-wave MEMS waveguide switch operating in a 40 % bandwidth between 500-750 GHz. The switch has an insertion loss better than 3 dB in the non-blocking state and isolation better than 15 dB in the blocking state. The discrepancy between the measured and simulated insertion loss is attributed to the combination of the insufficient gold thickness and the surface roughness on the waveguide sidewalls.

Acknowledgements. The research described herein is a collaboration effort between the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California, USA, under contract with National Aeronautics and Space Administration, and KTH Royal Institute of Technology, Stockholm, Sweden.

The contribution by KTH to this work has been funded through the European Research Council Consolidator Grant No. 616846, The Swedish Foundation for Strategic Research Synergy Grant Electronics SE13-007, and through a Nils and Hans Backmark scholarship.

References

[1] K.B. COOPER, and G. CHATTOPADHYAY, *Submillimeter-wave radar: solidstate system design and applications,* IEEE Microw. Mag.,**15**, (7), pp. 51-67, 2014.

[2] M. DANESHMAND and R.R. MANSOUR, *Multiport MEMS-Based Waveguide and Coaxial Switches*, IEEE Trans. Microwave Theory Tech., **53**, (11), pp. 3531-3537, November 2005.

[3] N. VAHABISANI, and M. DANESHMAND, *Monolithic millimeterwave MEMS Waveguide Switch*, IEEE Trans. Microw. Theory Tech., **63**, (2), pp. 340-351, Feb. 2015.

[4] Z. BAGHCHEHSARAEI, and J. OBERHAMMER, *Parameter Analysis of Millimeter-Wave Waveguide Switch Based on a MEMS Reconfigurable Surface*, IEEE Trans. Microw. Theory Tech., **61**, (12), pp. 4396-4406, Dec. 2013.

[5] U. SHAH et. al., *500-600 GHz RF MEMS Based Tunable Stub Integrated in Micromachined Rectangular Waveguide*, 2015 IEEE MTT-S Int. Microwave Symp. Dig., pp. 1-4, May 2015.

[6] U. SHAH et. al., *500-600 GHz Submillimeter-Wave 3.3 bit RF MEMS Phase Shifter Integrated in Micromachined Waveguide*, 2015 IEEE MTT-S Int. Microwave Sy. Dig., pp. 1-4, May 2015.

[7] F. BOUSSAHA, J. KAWAMURA, J. STERN, and C. JUNG-KUBIAK, *2.7 THz Balanced Waveguide HEB Mixer*, IEEE Trans. Microw. Theory Techn., **4**, (5), pp. 545-551, Sep. 2014.

[8] T. RECK, C. JUNG-KUBIAK, J. GILL, and G. CHATTOPADHYAY, *Measurement of silicon micromachined waveguide components at 500-750 GHz*, IEEE Trans. Terahertz Sci. Tech., **4**, (1), pp. 33-38, Jan. 2014.

RF Pad Optimization for a 140 GHz RF–MEMS Switch

S. TOLUNAY WIPF[1], A. GÖRITZ[1], M. WIETSTRUCK[1],
C. WIPF[1], M. KAYNAK[1,2]

[1]IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany
[2]Sabanci University, Orta Mahalle, Tuzla 34956 İstanbul, Turkey

Abstract. RF pads are designed based on IHPs 0.13 µm SiGe BiCMOS technology and measured in D–band (110–170 GHz). Using the optimized RF pad helps to eliminate the loss which is introduced by the coupling of the RF signal to the Metal1 (M1) ground shields. The extracted capacitance of the optimized RF pad shows a drop of 7 fF at 140 GHz. The goal of the RF pad optimization is to combine the new RF pad with a 140 GHz RF–MEMS switch in order to avoid the pad de–embedding procedure. The fabricated RF–MEMS switch with the optimized RF pads shows a low insertion loss of 0.68 dB at 140 GHz with an improvement of 0.45 dB compared to the same RF–MEMS switch with the not optimized standard RF pads.

Key words: RF–MEMS; BiCMOS; mm–wave; EM modeling; GSG; RF–pad

1. Introduction

SiGe technologies have become more attractive with the high performance of heterojunction bipolar transistors (HBTs) for millimeter–wave frequency applications [1]. The RF–MEMS switch integration into IHPs 0.13 µm SiGe BiCMOS process technology gives the opportunity to use low insertion loss and high isolation RF–MEMS switches together with high performance HBTs. This provides circuits with low attenuation, to be used in antenna switching matrices and phase shifters [2]. RF–MEMS switches in mm–wave circuits are lately realized and demonstrated for 94 GHz passive imaging systems and 140 GHz active radar systems [3].

RF pads are the essential elements to characterize RF– MEMS switches or any other RF–circuits, since they provide the direct access to the DUTs (device under test). The RF performance of the DUT should not be affected by the de–embedding of the RF pads; however accurate de–embedding of the RF pads is critical in the mm–wave frequency range [4]. Therefore the electromagnetic (EM) optimization of the RF pads itself is inevitable [5].

In this work, EM optimizations of RF pads for a 140 GHz targeted RF–MEMS switch are presented. The EM simulations are performed for standard and optimized RF pads and also both devices are fabricated, measured and the measurement results are compared. The switch, including the optimized RF pads, is monolithically integrated into IHP`s 0.13 µm SiGe BiCMOS process technology and provides 0.68 dB insertion loss and isolation of 32 dB at 140 GHz.

2. RF–MEMS Switch in 0.13 µm BICMOS Technology

IHPs RF–MEMS switch technology is embedded into the Back–end–of–line (BEOL) of the 0.13 µm SiGe BiCMOS technology. The developed RF–MEMS switch [6] consists of Metal4 (M4) high–voltage electrodes, a Metal5 (M5) RF–signal line, a TopMetal1 (TM1) movable membrane, and a TopMetal2 (TM2) plate with releasing holes. The TM2 plate is placed on top of the RF–MEMS switches to provide a wafer–level encapsulation packaging process. With this approach, no additional package will be required for the RF–MEMS switches as the devices will be encapsulated during the standard BEOL process. In this paper, the presented results of the RF-MEMS switches are in case of the uncovered encapsulation holes.

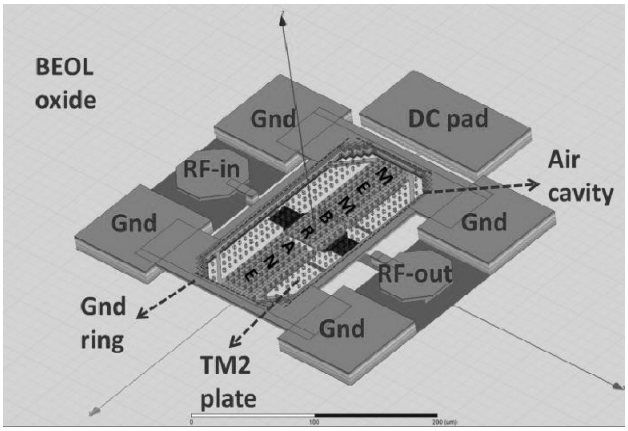


Fig. 1. EM model of a 140 GHz targeted RF–MEMS switch with its patterned TM2 plate, including standard RF pads.

3. RF–PAD Optimization

In order to optimize the GSG (Ground–Signal– Ground) pads of a 140 GHz targeted RF–MEMS switch, EM models were built up in Ansoft HFSS 3D FEM (Finite–Element–Method) solver. The goal of the RF pad optimization was not to

have a necessity to perform de – embedding since the performance including the pads will not be significantly different compared to a switch without RF pads. In the standard GSG pad configuration, Metal1 (M1) layer was patterned underneath the pads as a ground shield and the ground pads were connected to each other with metal and via stacks from M1 up to TM2 (Fig. 2–a). To achieve a minimum parasitic capacitance introduced by the RF pads, the optimized GSG pad (Fig. 2b) was designed only in TM2 layer. The optimized pad is created as a coplanar waveguide (CPW), with an 80 µm wide signal pad and 7 µm gap to the ground pads.

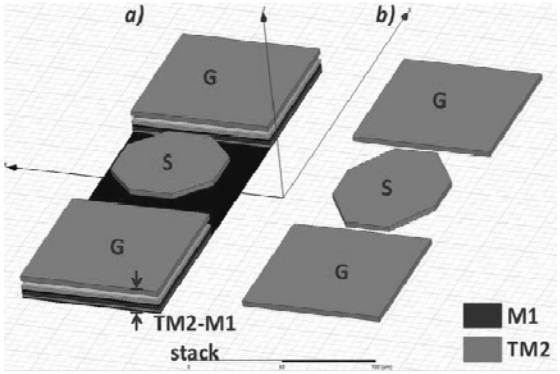


Fig. 2. RF GSG pad of the 140 GHz RF–MEMS switch (a) before and (b) after optimization.

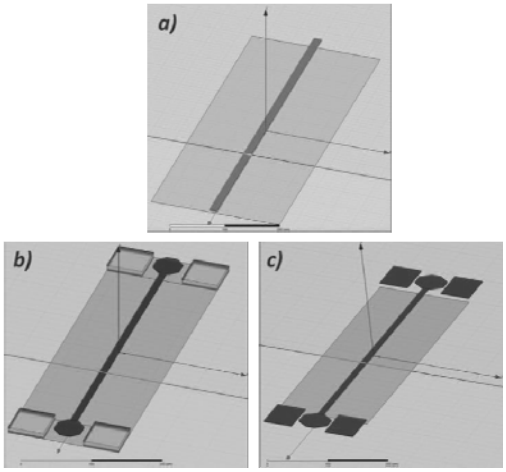


Fig. 3. EM simulations of a 50 ohm matched microstrip line (a) without RF pads, (b) with the standard RF pads and (c) the optimized RF pads.

During the EM optimization of the RF pad, different pad configurations were combined with a 50 Ω matched microstrip line and simulated (Fig. 3).

The designed microstrip line which consists of TM2 signal line and M1 ground shield, has a width of 15 µm, and a length of 730 µm. The EM simulation gives a loss of 0.47 dB at 140 GHz (Fig. 4–a). EM simulations also show that the impedance matching of the microstrip line significantly deviates by the standard RF pads (Fig. 4–b, c). With the standard RF pads, the impedance of the microstrip line decreases from 50.6 Ω to 20.8 Ω (Fig. 4–d). As a result of this mismatch, transmission line with the standard RF– pads shows 1.62 dB loss. On the other hand with the optimized GSG pads, the impedance of the microstrip line changes slightly, 3 Ω deviation at 140 GHz. The loss of the transmission line with the optimized RF–pads is 0.63 dB, which is only 0.15 dB higher than the transmission line loss without RF pads.

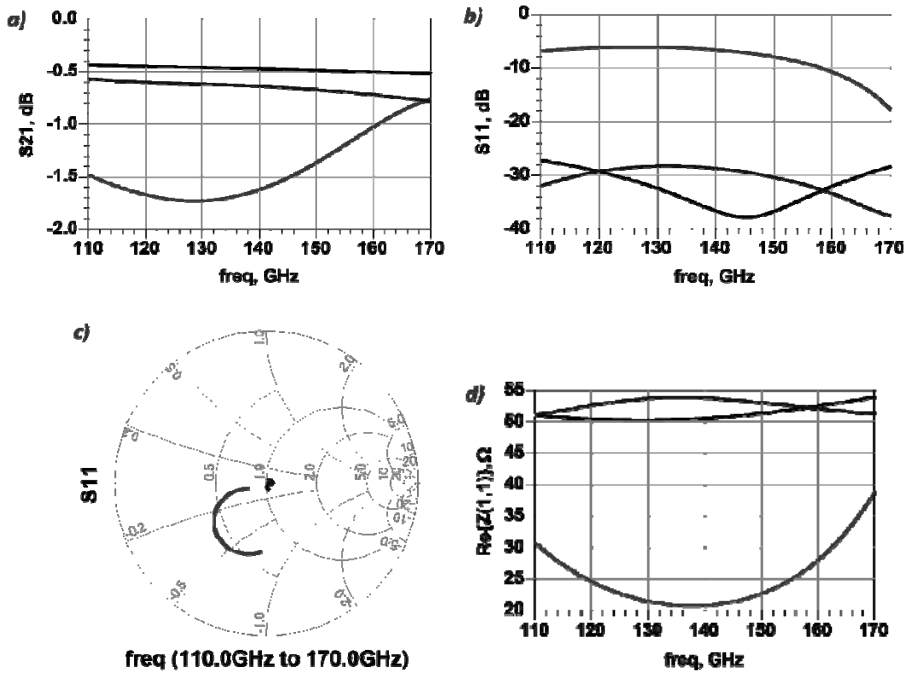


Fig. 4. S parameter (a, b, c) and characteristic impedance (d) comparisons of the 50 Ω matched microstrip line without RF pads (black), with the standard RF pads (red) and the optimized RF pads (blue).

After the optimization of the RF pads, both the standard and the optimized RF pads are fabricated in IHPs SG13 BEOL technology for further characterization. All two port on–wafer S–parameter measurements are

performed with a setup from Rohde & Schwarz, consisting of a 4 port ZVA24 as VNA / system controller and two ZVA170 Millimeter–Wave Converters from 110 to 170 GHz. Pad capacitances are extracted from equation (1) with conversion of the measured S parameters into Z parameters. With the new GSG pad configuration, the pad capacitance is reduced from 15 fF to 8 fF (Fig. 5), which is a reduction of ~45%.

$$C_{pad} = \frac{-1}{(2\pi f \cdot \mathrm{im}(Z(1,1)))} \tag{1}$$

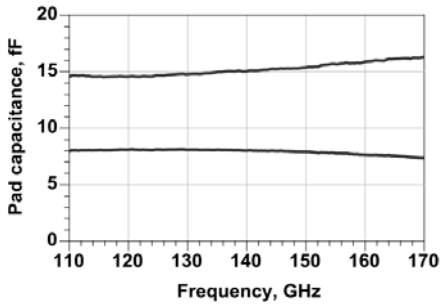


Fig. 5. Extracted capacitances of the standard (red) and optimized (blue) RF pads from S-parameter measurements.

Moreover to the RF–pad fabrications, the 140 GHz targeted RF–MEMS switch was simulated and fabricated together with the standard (Fig. 6a) and the optimized RF pads (Fig. 6b). The comparison of the simulated and measured RF–MEMS switches with both GSG pad configurations is shown in Fig. 7 with the apparent improvement of the insertion loss in the up–state. The measured S–parameter results of the RF–MEMS switch including the optimized RF pads provide 0.68 dB insertion loss and 32 dB isolation at 140 GHz.

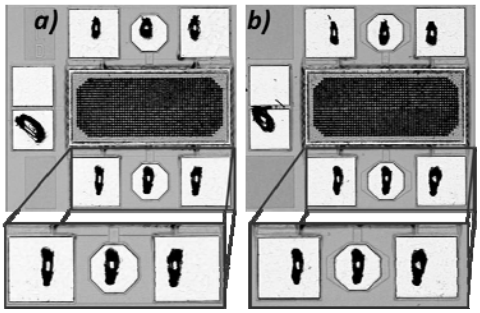


Fig. 6. The 140 GHz RF–MEMS switch with (a) the standard and (b) the optimized RF pads.

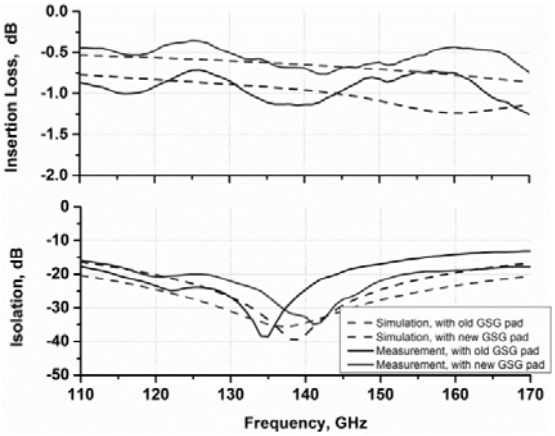


Fig. 7. EM simulation and S-parameter measurement comparisons of the RF-MEMS switch with the standard (blue) and optimized (red) GSG pad configurations.

4. Conclusion

An EM optimized RF–pad is designed and simulated together with a 50 Ω impedance matched microstrip line using Ansoft HFSS 3D FEM (Finite–Element–Method) solver. The optimized RF–pad shows ~45% reduction of the extracted pad capacitance compared to the standard RF pad with M1 ground shield. Finally, both the standard and the optimized RF–pads are combined with a 140 GHz RF–MEMS switch. The insertion loss of the 140 GHz RF–MEMS switch including the optimized RF pads is 0.68 dB at 140 GHz, which shows an improvement of 0.45 dB compared to the switch with the standard RF pads.

Acknowledgments. The authors thank to the team of the IHP pilot line for excellent support. This work was supported by the European Commission under the contract No. 288531– NANOTEC (www.project–nanotec.com).

References

[1] H. RUCKER, B. HEINEMANN, A. FOX, *Half–Terahertz SiGe BiCMOS technology*, Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2012 IEEE 12th Topical Meeting on , pp. 133–136, 16–18 Jan. 2012.

[2] T. CHALOUN *et al., Wide–angle scanning active transmit/receive reflectarray*, Microwaves, Antennas & Propagation, IET, **8 (**11), pp.811–818, August 19 2014.

[3] http://project–nanotec.com/

[4] B. ZHANG, Y. Z. XIONG, L. WANG, S. HU and J. L. W. LI, *On the De-Embedding Issue of Millimeter-Wave and Sub-Millimeter- Wave Measurement and Circuit Design*, in *IEEE*

Transactions on Components, Packaging and Manufacturing Technology, **2**(8) pp. 1361–1369, Aug. 2012.

[5] S. ALOUI, E. KERHERVE, J. B. BEGUERET, R. PLANA and D. BELOT, *Optimized pad design for millimeter-wave applications with a 65nm CMOS RF technology*, European Microwave Conference, 2009. EuMC 2009, pp. 1187–1190, Rome, 2009.

[6] S. TOLUNAY WIPF *et al*., *Thin Film Wafer Level Encapsulated RF– MEMS Switch for D–Band Applications*, accepted for European Microwave Week (EUMW) 2016.

Kapton Flexible Technology for V-band Applications

ZHENING YANG, ALEXANDRU TAKACS,
SAMUEL CHARLOT, DANIELA DRAGOMIRESCU

LAAS-CNRS, Université de Toulouse, CNRS, INSA, UPS, Toulouse, France

Abstract. This paper addresses the flexible Kapton technology for V-band applications. The proposed technology allows a fabrication accuracy down to 6 μm with insertion losses in the range of 0.5 dB/mm for coplanar waveguide lines at 60 GHz. Based on measurements results, the impact of humidity on the Kapton is quantified in the millimeter wave spectrum and V-band with the help of dedicated passive devices: ring resonator and antennas. An assembling process is also proposed in order to integrate active devices on flexible supporting Kapton board.

1. Introduction

Nowadays, there are increasing demands for flexible and wearable electronics. Also the targeted frequency dedicated for emerging applications increases. The millimeter spectrum and especially V-band are now addressed for short-range and high bit-rate communications. For such high frequencies, Kapton flexible substrate has become a trusted candidate. The Kapton exhibits: good RF and thermal properties, very good flexibility over a wide temperature range and good tolerance for many chemical solvents. This paper focus on the recent advances in the development of Kapton flexible technology for V-band applications. First, the Kapton technology is shortly described. Exhaustive investigations of the Kapton behavior in V-band including the quantified impact of the ambient humidity are presented in Section III and in Section IV, respectively. To the best of the authors' knowledge, the impact of humidity on the RF performances of passive devices fabricated by using Kapton technology was not yet experimentally characterized in V band. An assembling process of electronic chips by heterogeneous integration on flexible Kapton is also proposed in Section V.

2. Microfabrication Technology

All the structures presented in this paper were fabricated on a 127µm thick Kapton in the clean room by using a photolithography process. The technological process was optimized in order to obtain the best trade-off between the technological accuracy (line width or gap down to 6 µm can be obtained with a very good uniformity and reproducibility) that guaranty the millimeter wave performances and manufacturing cost that should be competitive. The Kapton is patterned on a PDMS-Si support for a negative photoresist spin coating. The metallization of electric pattern (Cr/Cu 50 nm/500 nm) is carried out by an electron beam physical vapor deposition (EBPVD) and then a surface finishing (gold immersion deposits) about a few nanometers is performed to prevent Cu from oxidizing. For V band applications the state of the arts of the available technologies are reported in Table I, The Kapton technology proposed in this paper exhibits very good technological accuracy and moderate RF loss, mandatory for V band applications.

Table I. Flexible Technologies for V band. CPW: CoPlanar Waveguide, MS: MicroStrip line

Substrate	Metallization	Technology	Accuracy	RF loss	Ref
PET	Silver	Inkjet	40 µm	0.4 dB/mm, CPW	[1]
Kapton	Silver	Inkjet	13 µm	1.5dB/mm, CPW	[2]
Kapton	Silver	Inkjet	35 µm	0.6 dB/mm, CPW	[3]
PEN	Silver	Inkjet	20 µm	Not reported	[4]
PerMX	Gold	Photolithography	5 µm	0.5 dB/mm, MS	[5]
LCP	Copper	Photolithography	85 µm	0.12 dB/mm, MS	[6]
Kapton	Copper	Photolithography	6 µm	0.5 dB/mm, CPW	

3. V-band Characterization of Kapton Technology

Multiple passive devices were selected as benchmark for this technology: a ring resonator, a microstrip patch antenna and a crossed slot dipole antenna. All above mentioned devices, represented in Fig. 1, Fig. 2 and Fig. 3, are appropriate for humidity tests due to their intrinsic sensitivity to dielectric property variation.

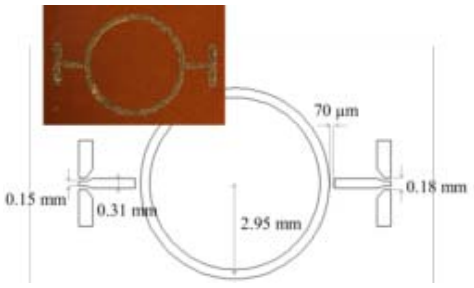


Fig. 1. (Color on line). Ring resonator: mains dimensions and the manufactured device.

The ring resonator is composed by a microstrip ring with the inner radius of 2.95 mm and two microstrip to grounded coplanar waveguide (GCPW) transitions that allows us to perform on-wafer measurements. The same GCPW to microstrip transition was used for the patch antenna. The width of the microstrip ring is 310 µm. There are two 70 µm gaps at the edges of the ring to couple the resonator without overload the test equipment.

The design of a crossed slot dipole antenna is inspired by a printed (coplanar stripline supported) crossed dipole antenna array [7] and the Babinet's principle. CPW feed dimensions of S = 170 µm and G = 12 µm were selected corresponding to the 50 Ohm GSG probe as shown in Fig. 3.

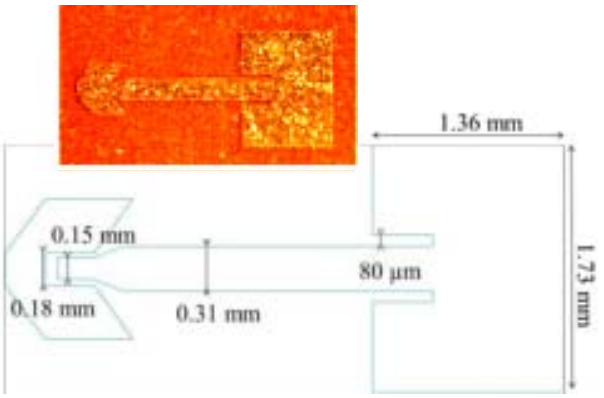


Fig. 2. (Color on line). Microstrip antenna: mains dimensions and the manufactured device.

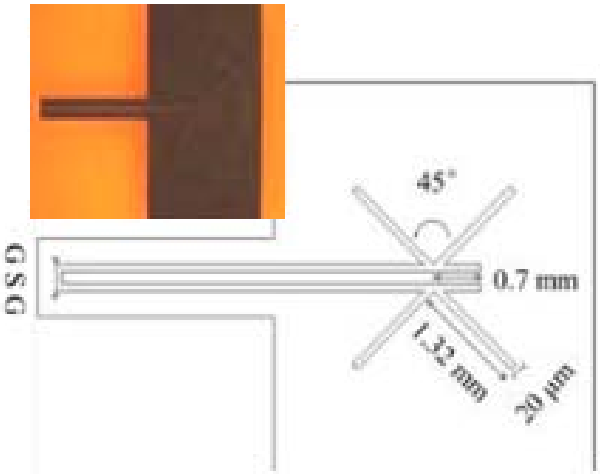


Fig. 3. (Color on line). Crossed slot dipole antenna: mains dimensions and the manufactured device.

4. V-band Humidity Measurement of Kapton

The humidity test method is based on IPC-TM-650 2.6.2.1 standard technique [8]. The test samples were firstly dry out in an oven for over 30 minutes at 150 °C, each of them was individually weighed immediately. Then the test samples were immersed in a crystallizing dish filled with deionized water for 12 hours (h). Each sample was removed independently from the water and sprays dried with nitrogen and weighed again. The same process was repeated for 24 h and 48 h respectively. The weight was increased with 1.64% after 12 h, 1.78% after 24 h and 1.81% after 48 h.

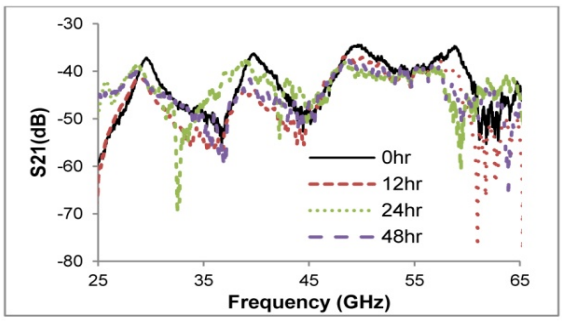


Fig. 4. (Color on line). Measured transmission coefficient of the ring resonator: initial state/0h (continuous black line), measure after 12h (red line, square dot), measure after 24h (green line, circular dot), measure after 48h (violet, dashed line).

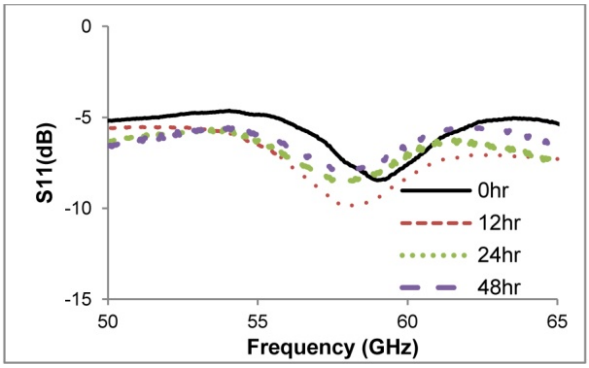


Fig. 5. (Color on line). Measured transmission coefficient of the microstrip patch antenna: initial state/0h (continuous black line), measure after 12h (red line, square dot), measure after 24h (green line, circular dot), measure after 48h (violet, dashed line).

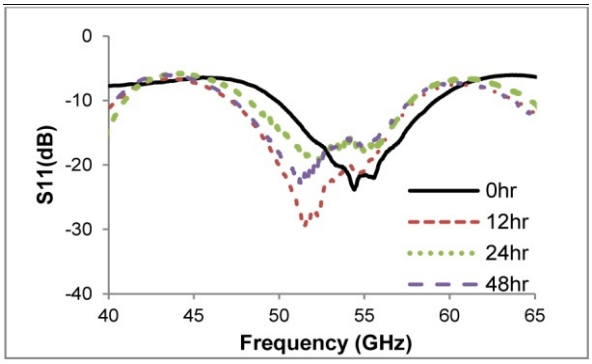


Fig. 6. (Color on line). Measured transmission coefficient of the crossed slot dipole antenna: initial state/0h (continuous black line), measure after 12h (red line, square dot), measure after 24h (green line, circular dot), measure after 48h (violet, dashed line).

The S-parameters measurements were carried out right after the weighing of the samples. Fig. 4 shows the results obtained for the ring resonator, the patch antenna and the crossed slot dipole antenna. The extracted values for the relative dielectric permittivity are reported in Table. II taking into account the associated tolerances.

Table II. Extracted dielectric constant and dielectric loss

Time	ε_r	Tolerance of ε_r	tanδ	Tolerance of tanδ
0 h	3.2	+/– 0.08	0.016	+/– 0.005
12 h	3.4	+/– 0.06	0.03	+/– 0.008
24 h	3.6	+/– 0.08	0.04	+/– 0.006
48 h	3.7	+/– 0.09	0.045	+/– 0.008

Fig. 5 and Fig. 6 show the measured reflection coefficient for the patch and the crossed slot antenna respectively. One can see that the frequency resonance is shifted to the lower frequency because the relative permittivity of the substrate was increased after water immersion as depicted in Table II. Also the S11 decreases because the dielectric losses increase due to water exposition. The input matching of the patch antenna is (only) –8.2 dB mainly due to the transition between microstrip and CPW line. This input matching should appear to be poor but it is not unusual for V-band antennas. For example the coplanar square monopole antenna proposed in [4] presents a measured S11 in the range of –11 dB at 58 GHz despite of the use of an 'intrinsic' CPW excitation. The second antenna (shown in Fig. 6) exhibits better performances: S11 < –20 dB in a 2 GHz bandwidth mainly due to its intrinsic CPW excitation and wideband behavior.

5. Flip Chip Assembling Technique

For the purpose of integration of different components on Kapton polyimide, different dummy circuits were mounted by using a flip chip technique [9] as followed: (i) gold stud ball bumping on chip, (ii) underfilling Kapton structure with an electrically non-conductive paste, (iii) chip with stud bump picked and placed to the Kapton structure by a flip-chip machine, (iv) thermal compression bonding. Four probe method was used to characterize the bumps resistivity as shown in Fig. 7. A resistance about 10 mΩ was measured for the gold bump, which proves a very good DC contact.

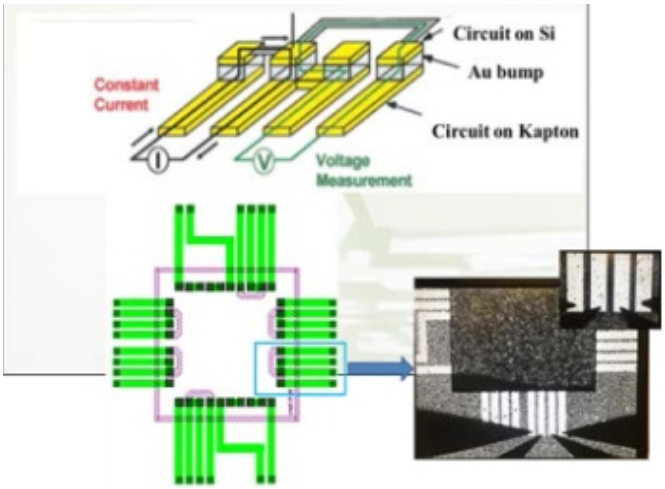


Fig. 7. (Color on line). Four probe method resistivity measurement.

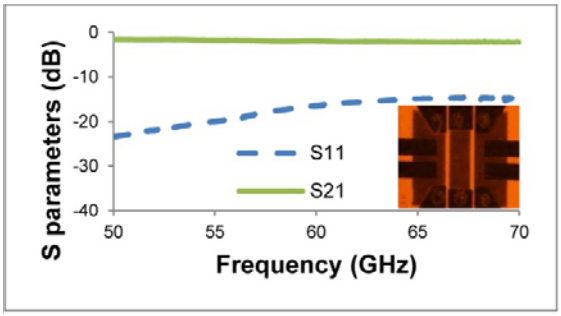
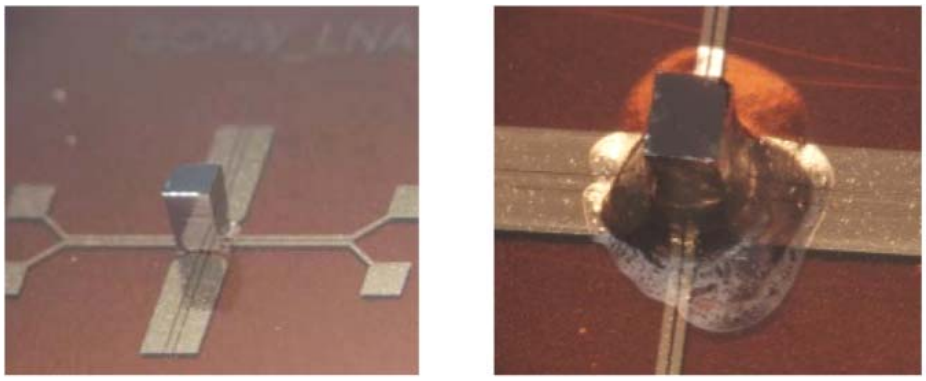


Fig. 8. (Color on line). Measured S-parameters of dummy CPW transmission line mounted on Kapton by using flip chip.

For the RF performance evaluation, firstly a 50 Ω dummy CPW transmission line on was mounted on Kapton as shown in Fig. 8). The measurement results of S-parameters show us a good RF performance. Then a home-designed V-band LNA manufactured by using 65 nm CMOS technology [10] was mounted on Kapton. Its dimension is about 400 µm x 400 µm large and 800 µm height. The pad size (both for RF and DC contacts) are 80µm x 80 µm. This chip is a 'worst case' from an assembling point of view because of its size (foot print of 400µm x 400 µm), aspect ratio (2) and pads size (80µm). The supporting Kapton structure is composed by 50Ω GCPW used as RF In and RF Out and DC pads as shown in Fig. 9.

During our first tests, only the interface between chip and substrate was filled with nonconductive paste (Epotek 353NDT, relative dielectric permittivity of 3.17 and dielectric loss tangent of 0.005 at 1 kHz), which is not robust enough. The chip was fallen apart from the substrate after several bending test. So we added some extra paste around the chip (Permabond UV625, relative dielectric permittivity of 4 at 1 MHz, dielectric loss tangent not known) to ensure the bonding. But this paste changes significantly the characteristic impedance of grounded coplanar line and degrades the RF performances of our LNA. The RF behavior of those pastes (Epotek 353NDT and Permabond UV625) was never investigated in V-band and we suppose that it is too lossy at such high frequencies. Works are under run in order to avoid this drawback by: (i) controlling the nonconductive paste deposition in order to minimize its impact of the CPW line, (ii) using a nonconductive paste with a better RF behavior.



a) b)

Fig. 9. (Color on line). LNA chip mounted on the Kapton supporting structure: (a) by using only Epotek 353NDT under the LNA chip, (b) by adding Permabond UV625 around the LNA chip

6. Conclusion

In this paper, several resonant passive devices were fabricated on Kapton flexible substrate. A standard humidity test was performed in V band. The experimental results demonstrates that the dielectric constant of the Kapton increases with maximum 15.6 % (up to 3.7 from 3.2 the initial value) and the dielectric losses increases with maximum 181% (up to 0.045 from the initial value of 0.016) when the Kapton structure were immersed in water after 48 hours. A limitation of the water absorption was also observed after 24 hours of the water immersion. The DC and RF measurements of dummy circuit mounted with flip chip technique show very promising results for a 3d heterogeneous integration.

References

[1] K. HETTAK, T. ROSS, R. JAMES, A. MOMCIU, and J. WIGHT, *Flexible plastic substrate-based inkjet printed CPW resonators for 60 GHz ISM applications*, 2014 44th European Microwave Conference (EuMC), pp.1194-1197, October 2014.

[2] S. SWAISAENYAKORN, P.R. YOUNG and M. SHKUNOV, *Characterization of ink-jet printed CPW on Kapton substrates at 60 GHz*, Antennas and Propagation Conference (LAPC), pp. 676-678, November 2014.

[3] M.M. BELHAJ, WEI WE, E. PALLECCHI, C. MISMER, I. ROCH-JEUNE and H. HAPPY, *Inkjet printed flexible transmission lines for high frequency applications up to 67 GHz*, 2014 44th European Microwave Conference (EuMC), pp. 1528-1531, October 2014.

[4] A. BISOGNIN, J. THIELLEUX, WEI WEI; D .TITZ, F. FERRERO, P. BRACHAT, G. JACQUEMOD, H. HAPPY, and C. LUXEY, *Inkjet Coplanar Square Monopole on Flexible Substrate for 60-GHz Applications*, Antennas and Wireless Propagation Letters, IEEE, **13**, pp. 435-438, 2014.

[5] S. SEOK and J. KIM, *Design, Fabrication, and Characterization of a Wideband 60 GHz Bandpass Filter Based on a Flexible PerMX Polymer Substrate*, Components, Packaging and Manufacturing Technology, IEEE Transactions, **3**, (8), pp. 1384-1389, August 2013.

[6] D. THOMPSON, O. TANTOT, H. JALLAGEAS, G.E. PONCHAK, M.M. TENTZERIS and J. PAPAPOLYMEROU, *Characterization of liquid crystal polymer (LCP) material and transmission lines on LCP substrates from 30 to 110 GHz*, Microwave Theory and Techniques, IEEE Transactions, **52**, (4), pp. 1343-1352, April 2004.

[7] A. TAKACS, H. AUBERT, S. FREDON and L. DESPOISSE, *Design and Characterization of Effective Antennas for K-band Rectennas*, 2015 9th European Conference Antennas and Propagation (EUCAP), pp. 1-4, 2015.

[8] https://www.ipc.org/TM/2-3_2-3-25-1.pdf.

[9] M.M. JATLAOUI, D. DRAGOMIRESCU, M. ERCOLI, M. KRÄMER, S. CHARLOT, P. PONS, H. AUBERT, and R. PLANA, *Wireless communicating nodes at 60 GHz integrated on flexible substrate for short-distance instrumentation in aeronautics and space*, International Journal of Microwave and Wireless Technologies, **4**, pp. 109-117, 2012.

[10] M. KRAEMER, D. DRAGOMIRESCU and R. PLANA, *A low-power high-gain LNA for the 60 GHz band in a 65 nm CMOS technology*, 2009 Asia Pacific Microwave Conference (APMC), pp. 1156-1159, December 2009.

Smart MEMS Piezo Based Energy Harvesting with Integrated Supercapacitor and Packaging

C. RUSU[1], A. ALVANDPOUR[2], P. ENOKSSON[3], T. BRAUN[4], S. TIEDKE[5], R. Dal MOLIN[6], G. FERIN[7], E. VIINIKKA[8], T. EBEFORS[9]

[1]Sensor Systems department, Acreo Swedish ICT, Sweden
E-mail: cristina.rusu@acreo.se
[2]Division of Integrated Circuits and Systems, ISY, Linköping University, Sweden
[3]Micro- and Nanosystems group, Chalmers Univ. of Technology, Gothenburg, Sweden
[4]Fraunhofer-IZM, Berlin, Germany
[5]aixACCT Systems GmbH, Aachen, Germany
[6]LivaNova, Clamart, France
[7]Vermon SA, Tours, France
[8]Spinverse Innovation Management Oy, Espoo, Finland
[9]Silex Microsystems AB, Järfälla, Sweden
E-mail: thorbjorn.ebefors@silex.se

Abstract. The smart-MEMPHIS project (H2020 RIA) has the ambition to combine new features of energy harvesting, energy storage and power management by miniaturization and innovative packaging technology to produce leadless pacemakers and structural health monitoring applications. The project will integrate several multi-functional technologies and nanomaterials; MEMS-based energy harvester, ultra-low-power ASIC, miniaturized energy storing supercapacitor, all heterogeneously integrated for cost effective 3D integration. The presentation will cover various aspects and requirements as well as the considered solutions for each module.

1. Introduction

IoT is one of the main drivers for technology development related to the main challenge of all smart devices-self-powering: a trillion sensors need power. A big percentage of IoT opportunities will not realise if batteries need to be changed often, they are placed in inaccessible places (*e.g.* inside bridges or building walls as for Structural Health Monitoring applications) or large quantities are required. However, energy harvester to be of any advantage, the applications would run on

ultra-low power, low data rate and low duty cycle. For these applications, miniaturization and low cost fabrication are needed.

Vibration piezoelectric energy harvesters convert mechanical strain into electrical energy. They have received much attention in the last 15 years, due to the simple configuration and high conversion efficiency as comparing to electrostatic and electromagnetic harvesters [1]. Utilization of Micro Electro Mechanical Systems (MEMS) technologies allows for a totally integrated system containing sensor, electronics, communication and energy source.

The International Technology Roadmap for Semiconductors has recognized energy efficient electronics as a key enabler for addressing the potential of spatially distributed and connected sensors [2]. We are interested in exploring and developing novel smart energy enabling technologies via MEMS-based energy harvesting technologies with a final goal of a system-on-chip or integrated component solutions. In particularly, designing novel structures in combination with piezoelectric MEMS technology for more energy efficient small-size electronic systems using autonomous power supply through new innovative technologies. However, the scaling remains an issue and the unfavourable scaling of power with miniaturization needs to be solved.

2. Energy Harvester System and Applications

A standard energy harvester system for a wireless sensor network consists of five main components: harvester, energy storage, microcontroller, sensor(s) and transceiver (Fig. 1).

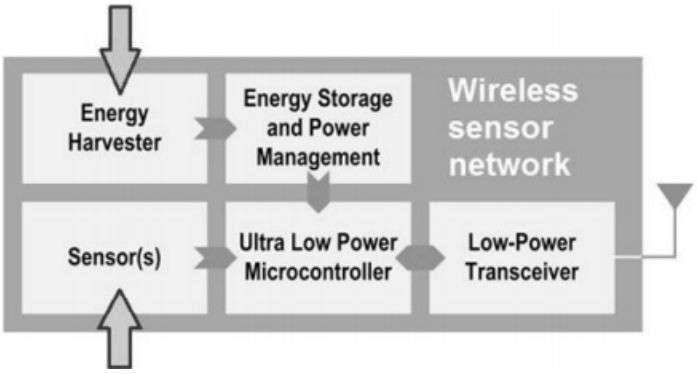


Fig. 1. Typical architecture of wireless sensor network.

Similar architecture is used also for the energy harvesting system developed within the Smart-MEMPHIS project [3] with focus on implantable pacemakers and aircrafts (Fig. 2).

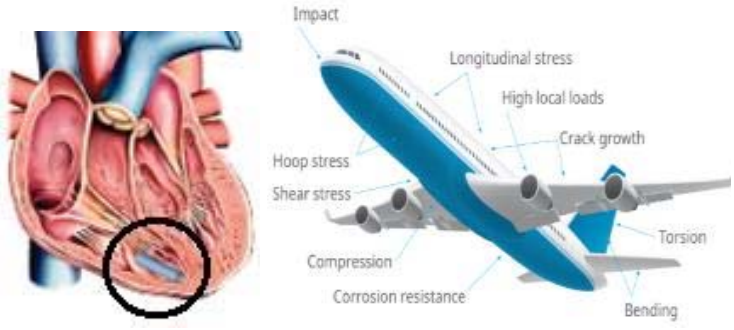


Fig. 2. (Color on line) Leadless pacemaker (left, © LivaNova, reproduced with permission) and Structural Health Monitoring (SHM) for aeronautical application (right).

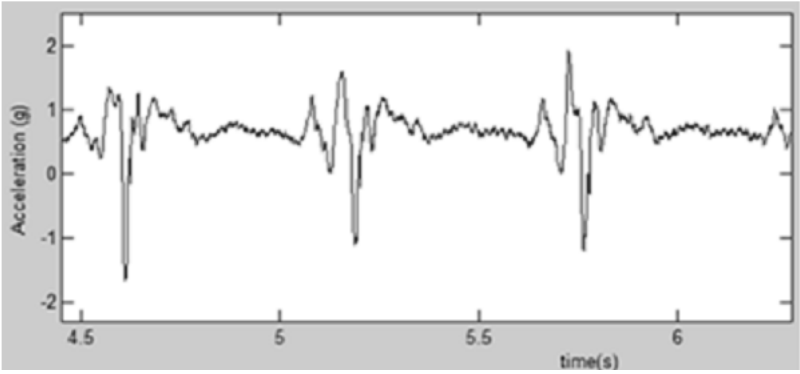


Fig. 3. Heartbeat waveform.

Smart implantable medical devices will require a solution to the problem of device longevity. While for SHM, the monitoring of the changes in material complex structures (*e.g.* micro-cracks in aircraft wings), requires at present many various sensors to collect data. So, there is a need for smart autonomous wireless acoustic sensors for aeronautical SHM applications.

For the leadless pacemaker, the energy sources inside the body, near the heart looks as shown in Fig. 3. For the harvester we are using the heart's mechanical vibration as transduction.

The smart-Memphis energy harvester is based on MicroElectroMechanical systems (MEMS)-based thin-film piezoelectric mechanism that is more attractive

for converting mechanical energy into electrical energy at small dimensions (mm^3 scale).

3. Piezoelectric Material Deposition

PZT (Lead Zirconate Titanate) is a piezoelectric material with compelling properties:

- Piezoelectric
  - Mechanically stressed => Develops voltage
  - Voltage applied => Physically changes shape
- Dielectric
  - Large dielectric constant
- Pyroelectric
  - Temperature change => Develops voltage
- Ferroelectric
  - Spontaneous electric polarization

There are two main ways of depositing PZT films: sol-gel and sputtering. For smart-Memphis we use sol-gel deposition (Fig. 4) because it is a low-cost technology, has high deposition rate, allows for excellent thickness uniformity, has less defects and high breakdown voltage. SEM images of typical PZT layers deposited by Silex are shown in Fig. 5 and Fig. 6.

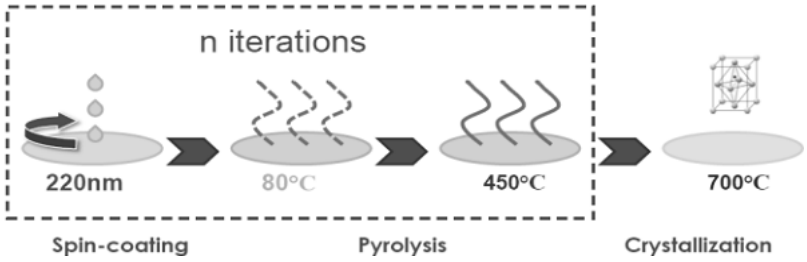


Fig. 4. Schematic of PZT sol-gel deposition.

Industry-benchmark levels for figure of merit of Silex PZT are:

– Piezoelectric effect e_{31}: -15 C/m^2 with high wafer Uniformity
– Young's modulus: 75GPa
– Relative permittivity ε_r: 1200 (tunable from 700 to >1400)
– Breakdown voltage: 80–130 V/μm depending on PZT type
– Leakage current: < 200 nA/cm^2
– Reliability testing evaluation in progress with good preliminary results.

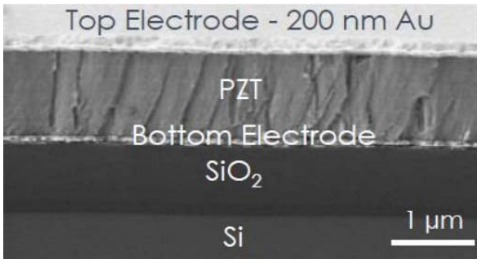


Fig. 5. 1.2 µm <100> PZT with only 6 layers.

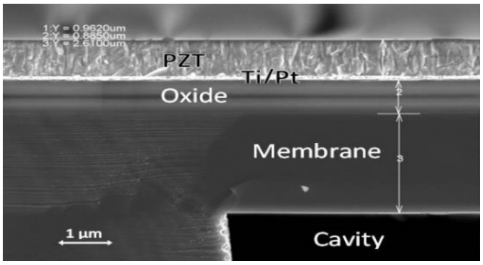


Fig. 6. PZT on Cavity SOI substrate.

4. Piezoelectric Material Characterization & Poling

A poling setup has been designed by AixACCT Systems Gmbh allowing for non-destructive poling and testing on wafer level (Fig. 7) as well as on device level. A poling set-up for fast heating and cooling of 1inch samples with integrated measurement for deflection measurement of MEMS structure has been also developed. These allow for enhanced characterization of thin film and device by determination of e_{31} on wafer level, also heating systems for piezoelectric thin film test systems and implementing of in-situ e_{31} measurements during poling.

5. MEMS Harvester Structure Design & Characterization

Energy flow of piezoelectric harvester has tree primary steps: capturing the mechanical stress from the available source, converting the mechanical energy into electrical energy with the piezoelectric transducer, and processing and storing the generated electrical energy. For each of these steps, there are losses involved; for mechanical excitation, mechanical to electrical conversion, and electrical conversion. The harvester design (by Acreo Swedish ICT) aims to decrease these losses via harvester geometry and its packaging, via proper modelling of the physical-mechanical to electrical transduction using analytical models and finite

element simulation (Comsol, Ansys). The MEMS harvester works in d_{31} mode where the electric field is perpendicular to the strain direction (Fig. 9).

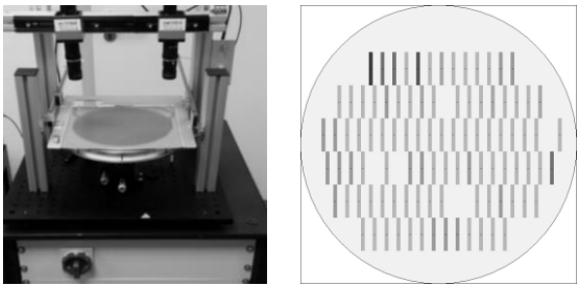


Fig. 7. Prototype full wafer poling (left) and Non-destructive poling and testing on wafer level (right).

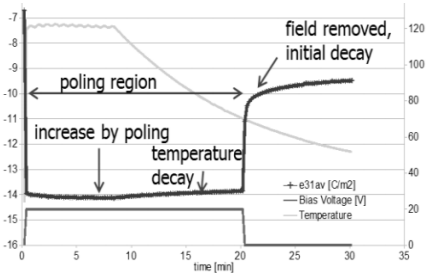


Fig. 8. *In-situ* measurement of e_{31} during temperature poling.

For the harvester characterization, Acreo uses a combination of Laser Doppler vibrometer, shaker and vacuum chamber to obtain information on mechanical characteristics, piezo-mechanical coupling, damping and losses (air and vacuum) and verification of harvester model.

5. Super Capacitor

The supercapacitor is a storage device for the harvested energy and consists of electrodes, separators and electrolytes. Novel materials are explored for the different parts of the supercapacitor. Material requirements for electrodes are porosity, surface area, mechanical stability, electrical conductivity, electrochemical stability. For the electrodes, especially carbon nanostructures synthesized by CVD (chemical vapor deposition) and electrospun cellulose carbonized by pyrolysis are developed. Specifically, 3D structured carbon nanofiber / MnO_2 composite material (NCNF / MnO_2) exhibits the best performance with high specific capacitance (108.6 F/g @ 0.5A/g) and excellent power capability (84.3 F/g @ 15 A/g).

The separator uses glass fiber with high thermal stability up to 600°C, excellent mechanical property and high uptake of different electrolytes. The electrolyte is a high temperature ionic liquid (EMIM Ac) enables high working voltage window up to 1.5 V and increases the energy density to 21.1 Wh/kg. Temperature durable PVA / H_3PO_4 gel electrolyte with reduced leakage risk and high package capability. The device with gel electrolyte can deliver 82 mF after high temperature exposure.

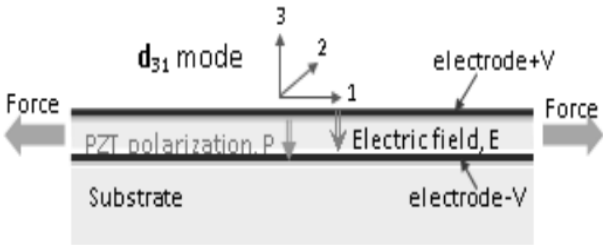
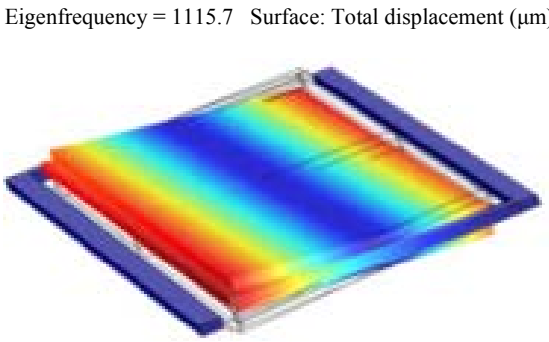


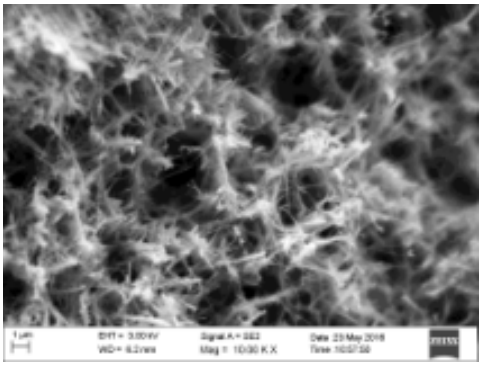
Fig. 9. Applied force, strain, electric field and polarization for the d_{31} mode of operation.



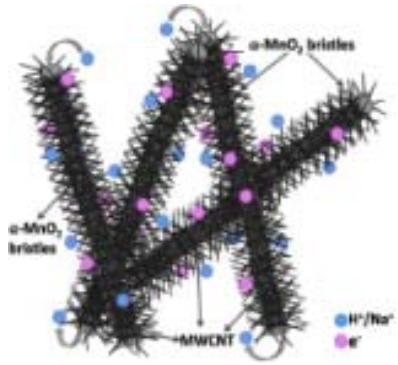
(a)

(b)

Fig. 10. (Color on line). MEMS harvester simulation (a) and image of shaker (b).



(a)



(b)

Fig. 11. (Color on line). MnO_2 growth on Carbon Nano Fiber matrix; (a) SEM image, (b) schematic.

7. Power Management Unit

Ultra-low-power integrated power management unit (PMU) for the leadless pacemaker (Fig. 12) contains the piezoelectric-harvester interface circuits (rectifier) for power-transfer, DC-DC power conversion, voltage regulation and control circuitry. The key goals and challenges are the efficient extraction of very low power-levels (in the μW range) and also ultra-low-power / low-voltage IC design.

The energy consumption bottlenecks are the Communication unit (RF standard, protocols), Memory unit (low-voltage RAM), Sensor interfaces (ADCs and drivers), Power management unit (efficiency) and Controller unit. The first generation test chip in 0.18μm CMOS technology with high-voltage option including reconfigurable rectifier and DC/DC conversion is under characterization.

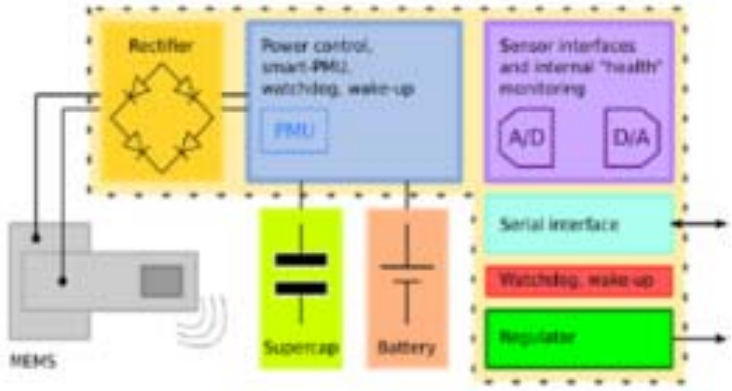


Fig. 12. Schematic of ultra-low-power integrated power management unit for energy harvesting.

8. Packaging Concept

The above components; the stress sensitive MEMS harvester, the PMU / ASIC and the energy storage need to be packaged (Fig. 13a) and integrated into the leadless pacemaker and structure health monitoring. The highly miniaturized packaging technology is based on Fan-out Panel Level Packaging (Fig. 13b) and Package-on Package (PoP).

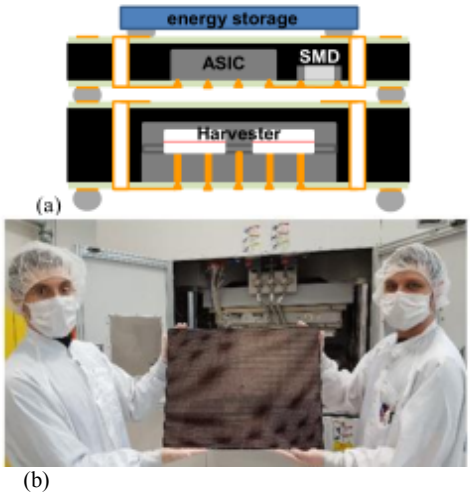


Fig. 13. (a) Schematic of smart-Memphis packaging concept and (b) Fan-out Panel Level Packaging processing on 24“x18“

9. Conclusion

The smart-Memphis project has many challenges for all components of the system:

- Energy harvesting from vibrations (TRL2 → TRL5) Challenge: Low frequency (10Hz), small movements, and small size Approach: sol-gel PZT process and smart harvester design.
- Energy storage (TRL2 → TRL4-6) Challenge: Rechargeable, energy density, maturity Approach: Functionalisation of electrode materials.
- Tailored ASICs (TRL2 → TRL6) Challenge; Low energy consumption and small size Approach: Efficiency and very low static energy consumption.
- Packaging (TRL3 → TRL6-7) Challenge: Size and reliability Approach: Flat panel packaging, either 2D / 3D.

Acknowledgements. Smart-MEMPHIS project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 644378.

References

[1] S. ROUNDY *et al.*, Energy scavenging for wireless sensor networks-with special focus on vibrations; Kluwer Academic Publishers, Boston MA. ISBN 1-4020-7663-0, 2003.
[2] Jwww.itrs.net/.
[3] http://www.smart-memphis.eu/.

Analysis of dielectric charging assessment through up-state capacitance-voltage characteristic in MEMS capacitive switches

M. KOUTSOURELI*, D. BIRMPILIOTIS, L. MICHALAS and G. PAPAIOANNOU

Physics Department, University of Athens, 15784 Panepistimioupolis, Athens, Greece, Phone: +30 2107276722,
*Email: mkoutsoureli@phys.uoa.gr.

Abstract. The present paper aims to provide a better approach on the analysis of pull-up capacitance-voltage characteristic of MEMS capacitive switches by introducing an analytical model that takes into account the case of a real device, where the charge is not uniformly distributed at the surface of the dielectric film and the switch armatures are not parallel. The proposed model allows the use of capacitance- voltage characteristic's derivative, which slope is directly related to the device mechanical characteristics and the stress induced during charging. The application of the model on a MEMS switch with a parabolic up-state capacitance-voltage characteristic during charging and discharging processes allows the draw of conclusions on the charging and the mechanical performance of the devices.

1. Introduction

Capacitive RF MEMS switches are very promising devices for RF applications due to their small size, weight and possibility to be integrated in ICs. Despite these advantages reliability problems still hinder their commercialization, the most important being the effect of the dielectric charging that causes erratic device behavior [1].

The dielectric charging of the insulating film in capacitive MEMS switches has been intensively investigated by employing various assessment methods in both MEMS and MIM (Metal-Insulator-Metal) devices [2,3,4]. The lifetime of capacitive switches has been determined by monitoring the number of cycles to stiction or the shift of pull-in voltage under different actuation voltage profiles, device temperatures [1,5,6,7] and ambient conditions [8]. Meanwhile, a different approach has been proposed J. Wibbeler *et al*. [9] for the calculation of dielectric

film's surface net charge in capacitive MEMS switches with parallel armatures. The latter approach has been adopted in [10, 11, 12, 13] and [14] where a fast algorithm was derived for the calculation of the dielectric film charge density. The method in [9] was based on the recording of the up-state capacitance-voltage (C-V) characteristic, determining the bias for the minimum capacitance, calculating the net surface charge and monitoring the evolution of the net charge during charging or discharging processes. The advantage of this method arises from the fact that it is not affected by the moving armature creep, which decreases the device pull-in voltage and therefore does not allow the accurate calculation of net charge from the shift of pull-in or pull-out voltages X.

Rottenberg *et al*. [15] has proposed a more realistic model for the case of switches with non-parallel armatures and distributed charge across the surface of the dielectric film. Assuming small capacitance variance, the model was applied to the calculation of the long-term discharge current through the dielectric film [16] and to study the contacted and induced charging as well as the discharging current flowing through the dielectric film in capacitive switches during up-state [17]. Beyond these the observed broadening or narrowing of the up-state C-V characteristic and its continuous variation during charging or discharging has not received the appropriate consideration and obviously it has not been exploited for extraction of additional information related to device degradation.

The aim of the present paper is to derive analytical equations for the up-state capacitance-voltage characteristic of real MEMS capacitive switches with non-planar electrodes and distributed trapped charges, which will improve the characterization methodology and allow the obtaining of a better insight on the dielectric charging assessment. Devices with symmetric up-state C-V characteristics, for small displacement from equilibrium state, illustrate the importance of the proposed model and the related methodology. The experimental results are used to draw conclusion on the device electrical and mechanical performance.

2. Theoretical Model

In order to investigate dielectric charging phenomena in the present work we adopted the device model proposed in [15], presented in Fig.1, which includes a fixed non-flat metal plate of area A covered with a dielectric film of uniform thickness and a dielectric constant ε_r. Above it a rigid but non-flat moveable metal plate is fastened with a linear spring k to a fixed wall above the dielectric layer at a rest position $d_0(x,y)$. When a DC voltage V is applied between the two plates, the moving plate is displaced by Δ from its rest position to a new position $d(x,y)$. In such a device the movable electrode displacement (Δ) is given by:

$$\Delta = \frac{A}{2k\varepsilon_0}\left[\left(V_{\mu\alpha} - \mu\beta\right)^2 + V^2\sigma_\alpha^2 + \sigma_\beta^2 - 2V\,\mathrm{cov}_{(\alpha,\beta)}\right] \quad (1)$$

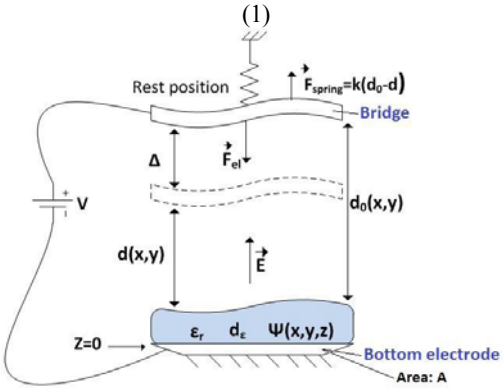


Fig. 1. Schematic model of a MEMS device with non-uniform trapped charge and air-gap distribution

where μ, σ^2, and cov are the mean, the variance and the covariance, respectively, of the capacitance per unit area [$\alpha(x,y,\Delta)$] and the induced charge density [$\beta(x,y,\Delta)$] at the armature area due to charges trapped at the dielectric. The relationships of $\alpha(x,y,\Delta)$ and $\beta(x,y,\Delta)$ are analytically given in [15].

According to the analysis in [18], for a small displacement of the moving electrode ($\Delta << d_0(x,y)$) from the equilibrium position and neglecting the higher order terms, the capacitance per unit area distribution $\alpha(x,y,\Delta)$ can be written as:

$$\alpha(x,y,\Delta) = \frac{\varepsilon_0}{d_0(x,y) + \frac{d_\varepsilon}{d_r}}\left[1 + \frac{\Delta}{d_0(x,y) + \frac{d_\varepsilon}{d_r}}\right] = \alpha(x,y,0) + \alpha(x,y,0)^2 \cdot \frac{\Delta}{\varepsilon_0} \quad (2)$$

The switch measured capacitance, C(V), can be then calculated by integrating Eq.2 over the active area and the substitution of Δ from Eq.1 leads to:

$$C(V) = A_{\mu\alpha} + \frac{A^2}{2k\varepsilon_0^2}\left(\mu_\alpha^2 + \sigma_\alpha^2\right)\left[\left(V_{\mu\alpha} - \mu\beta\right)^2 + V^2\sigma^2\alpha^2 + \sigma_\beta^2 - 2V\,\mathrm{cov}_{(\alpha\beta)}\right] \quad (3)$$

where μ_α and σ_α are the mean value and the variance of the capacitance per unit area, measured at applied bias V. The derivative of capacitance is thus given by:

$$\frac{dC(V)}{dV} = \frac{A^2}{k\varepsilon_0^2}\left(\mu_\alpha^2 + \sigma_\alpha^2\right)\left[\left(\mu_\alpha^2 + \sigma_\alpha^2\right)V - \mu_\alpha\mu_\beta - \mathrm{cov}_{(\alpha\beta)}\right] \quad (4)$$

Eq.4 indicates that there is a linear dependence of MEMS up-state capacitance derivative on the applied voltage, with slope S and abscissa V_0:

$$S = \frac{A^2}{k\varepsilon_2^0}\left(\mu_\alpha^2 + \sigma_\alpha^2\right)^2 \quad (5)$$

and

$$V_0 = \frac{\mu_\alpha\mu_\beta + \mathrm{cov}(\alpha,\beta)}{\mu_\alpha^2 + \sigma_\alpha^2} \quad (6)$$

The above analysis clearly shows that in the general case of non-flat electrode switches the slope must be proportional to $\left(\mu_\alpha^2 + \sigma_\alpha^2\right)$ and inverse proportional to the magnitude of spring constant k, when the displacement of the moving electrode from the equilibrium position is small. Thus the evolution of slope S, during a stress as well as a recovery test process, will provide valuable information on the deformation of the electrode, as long as the variance of the moving electrode remains practically constant for small displacements close to equilibrium. On the other hand, it may provide insight on the presence of a non-planarity that may give rise to uncontrolled stress gradient and the formation of a dipole across the dielectric film, due to contacted or field emission charging. In such a case, the up-state capacitance variance will significantly vary with applied bias leading to a non-linear derivative and hence non-constant S.

3. Experimental Details

The switches used in the present work are bridge-type capacitive switches fabricated with a standard photolithographic process on high resistivity silicon substrates on top of which a 3 μm SiO_2 film was deposited. The silicon nitride (SiN_X) dielectric film was grown on top of an electroplated gold (Au) layer with HF (13.56 MHz) PECVD method at 200 °C and the thickness of the film is 250 nm. XPS measurements revealed that the stoichiometry of the investigated silicon nitride (SiN_X) films is $x = N/Si \approx 1.04$. The membrane consisted of an evaporated titanium (Ti) – gold (Au) seed layer followed by a gold (Au) electroplated layer

of 2.0 μm thickness. A 2.2 μm sacrificial layer was used to determine the up-state position of the bridge. The active area of the switches is 2.5×10^{-5} cm^2 and the pull-in voltage is $V_{pull\text{-}in}$= 20 V.

The contacted charging was performed under a bias of 30 V and the up-state C-V characteristics were monitored after each successive stress step or after the end of stress process with the aid of a Boonton 72B capacitance meter with a resolution of 0.2 fF, while sweeping the voltage in 50 mV steps. The acquired bias was applied to the transmission line by a 6487 Keithley voltage source picoampere meter. The duration of each stress step was 30 s while the total stress time was 5 min. The discharging process was monitored for time length up to 10^4 s. Finally, all measurements have been performed under vacuum in a cryostat, with prior 2 hours annealing at 140 ^{0}C in order to minimize interference from humidity [3].

4. Results and Discussion

The typical up-state C-V characteristic of a MEMS capacitive switch, according to Eq. 3, must exhibit a parabolic shape for small moving armature displacement from equilibrium state ($\Delta<<d_0$) and the shape of the parabola is expected be determined by the device mechanical properties solely. Due to charging, the parabola will shift across bias axis with the magnitude of the shift determined by the net charge, μβ, while the value of minimum capacitance may increase or decrease

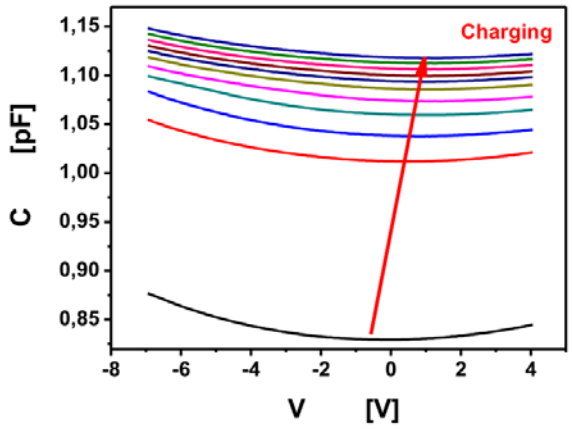


Fig. 2. (Color on line). Parabolic up-state C-V characteristics of a switch during charging.

with respect to the ideally uncharged film depending on both the charge distribution

variance and the mechanical properties degradation.

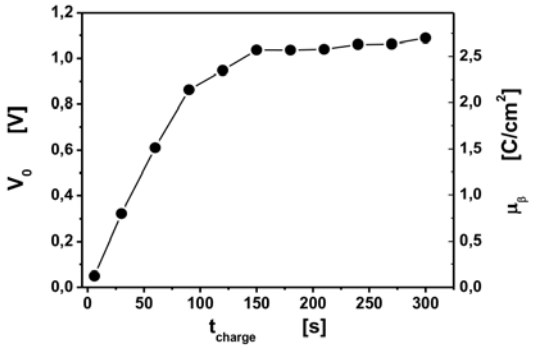


Fig. 3. The shift of bias V_0 during charging and the corresponding values of equivalent surface charge density μβ calculated assuming that we have a uniform charge distribution and that the switch electrodes are parallel.

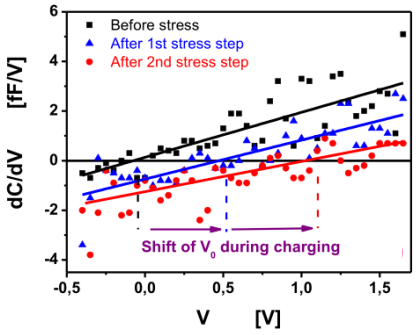
Figure 2 shows the up-state parabolic C-V characteristics of a switch that exhibit a good agreement with the theoretical one, predicted by Eq. 3. The C-V characteristics shift to positive voltages after each successive stress step with a positive bias and the shift of bias V_0 for capacitance minimum is presented in Fig. 3. Assuming that we have a uniform charge distribution ($\sigma_2 = 0$) and that the switch electrode plates are parallel ($\sigma_2 = 0$), which leads to zero covariance of parameters α and β (covα,β = 0), we have also calculated the equivalent charge density μβ from Eq. 6 after each successive stress step and the results are shown in the right axis of Fig.3.

The minimum capacitance is found to increase with stress (Fig. 2), a behavior that has been reported to arise from the increase of charge distribution variance [15]. Here it must be pointed out that according to the proposed model, taking into account Eq. 6, the capacitance minimum measured at V_0 is given by:

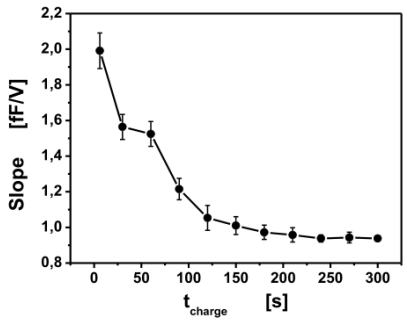
$$C_{\min}(V_0) = A\mu_\alpha + \frac{A^2}{2k\varepsilon_0^2}\left[\left(\mu_\alpha^2 + \sigma_\alpha^2\right)\left(\mu_\beta^2 + \sigma_\beta^2\right) - \left(\mu_\alpha\mu_\beta + \mathrm{cov}_{(\alpha,\beta)}\right)\right] \qquad (7)$$

revealing a complex dependence on the parameters that are introduced to describe the deviation from the ideal case. The derivative of the C-V characteristics before and after two charging steps are plotted in Fig. 4a. In spite of the measurements' noise the derivative exhibit a linear relation with the applied voltage, as shown by applying linear fit to our experimental results. A fast decrease of the C-V characteristic's derivative slope S for the same switch as the charging process evolves with time is presented in Fig. 4b. Assuming a short stress time, we may attribute this behavior to uncontrolled stress gradient and to the formation of a non-uniform charge distribution, the scale of which may give rise to the formation of a dipole across the dielectric film. This behavior, according to Eq. 5, may affect

the nominator $\left(\mu_\alpha^2+\sigma_\alpha^2\right)$ and taking into account that the minimum capacitance



a)



b)

Fig. 4. (a) Typical capacitance derivatives before and after two stress steps and (b) the dependence of the slope S on the charging time.

increases with stress time (Fig. 2), we are led to the conclusion that the switch may exhibit a large capacitance variance σα that decreases significantly during stress. We also mention that the decrease of S due to an increase of the spring constant k cannot be overruled, because stress induced hardening, *i.e.* increase of dynamic spring constant with stress time, has been observed in ultrafine crystalline nickel devices [19] and also alternating hardening and softening behavior has been reported until fracture in Au films [20].

The discharge process for the same switch has been also investigated by monitoring the shift of the up-state C-V characteristics during discharge and the previous theory model has been applied. The up-state C-V characteristics are parabolic and the minimum up-state capacitance decreases with time during discharge (Fig. 5a). Moreover, it has been found that the C-V characteristic's derivative slope S decreases with discharging time (Fig. 5b). This behavior is similar to the one observed during charging but the decrease rate is much lower. As already mentioned, the decrease of slope may result from a decrease of the nominator $\left(\mu_\alpha^2+\sigma_\alpha^2\right)$ (Eq. 5), which arises from the decrease of minimum

capacitance (Fig. 5a) and/or the decrease of σ_α^2 due to the charge draining by the bottom electrode and the redistribution across the surface of the dielectric film [11]. Finally, the gradual recovery of the mechanical properties cannot be ignored.

6. Conclusion

An analytical model for the up-state capacitance-voltage characteristic has been presented for the case of a real MEMS capacitive switch with non-uniform charge and capacitance distributions. The derivative of the C-V characteristic allows the separation of the parameters involving mechanical properties and electrical ones, that is the charging of the dielectric film. The application of the model to switches with smooth parabolic C-V characteristics revealed that the slope

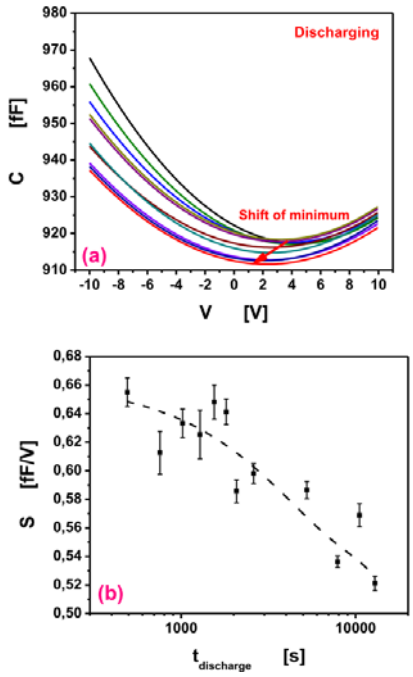


Fig. 5. (a) Up-state C-V characteristics of a switch during discharge and (b) the dependence of the slope S on the discharging time (dashed line shows the trend of our data).

of the C-V characteristic derivative decreases with stress time suggesting a decrease of capacitance variance or rather an increase of spring constant, the latter being presently under further investigation. The slope of the C-V characteristic

derivative has been also found to decrease during discharge, but the decrease in this case is much lower. Finally, considering all these, we conclude that the slope of the C-V characteristic's derivative in MEMS capacitive switches requires further investigation in order to extract the important information on the device degradation.

Acknowledgements. The first author, Matroni Koutsoureli, would like to thank *IKY Fellowships of Excellence for Postgraduate Studies in Greece – Siemens Program* that takes place in the framework of the Hellenic Republic – Siemens Settlement Agreement.

References

[1] G.M. REBEIZ, *RF MEMS theory, design and technology* Hoboken, Willey, New Jersey, USA (2003) 185-215.

[2] G. PAPAIOANNOU, *Dielectric Charging in Advance F MEMS* E. S. Lucyszin, Cambridge University Press (2010) 140-187.

[3] G. PAPAIOANNOU and R. PLANA, *Physics of Charging in Dielectrics and Reliability of Capacitive RF-MEMS Switches* in Advanced Microwave and Millimeter Wave Technologies Semiconductor Devices Circuits and Systems, Ed. M. Mukherjee (2010) 275-301.

[4] C. GOLDSMITH, J. EHMKE, A. MALCZEWSKI, B. PILLANS, S. ESHELMAN, Z. YAO, J. BRANK AND M. EBERLY, *Lifetime characterization of capacitive RF MEMS switches*, IEEE MTT-S International Microwave Symposium Digest. **1** (2001) 227 – 230.

[5] W.M. VAN SPENGEN, R. PUERS, R. MERTENS AND I. DE WOLF, *A comprehensive model to predict the charging and reliability of capacitive RF MEMS switches*, J. Micromech. Microeng. **14**, (2004) 514-521.

[6] C.L. GOLDSMITH, D.I. FOREHAND, Z. PENG, J.C.M. HWANG AND J.L. EBEL, *High-cycle life testingof RF MEMS switches*, IEEE International Microwave Symposium (MTT-S) (2007), 1805 – 1808.

[7] P. CZARNECKI, X. ROTTENBERG, P. SOUSSAN, P. EKKELS, P. MULLER, P. NOLMANS, W. DE RAEDT, H.A.C. TILMANS, R. PUERS, L. MARCHAND AND I. DE WOLF, *Effect of substrate charging on the reliability of capacitive RF MEMS switches,* Sensors and Actuators A (2009) 261–268.

[8] J. WIBBELER, G. PFEIFER, M. HIETSCHOLD, *Parasitic charging of dielectric surfaces in capacitive microelectromechanical systems (MEMS),* Sensors and Actuators A (1998) 74-80.

[9] R.W. HERFST, H.G.A. HUIZING, P.G. STEENEKEN and J. SCHMITZ, *Characterization of dielectric charging in RF MEMS capacitive switches*, in Proc. IEEE Int. Conf. on Microel. Test Struct. (ICMTS) (2006) 133-136.

[10] R.W. HERFST, P.G. STEENEKEN and J. SCHMITZ, *Time and voltage dependence of dielectric charging in RF MEMS capacitive switches*, in Proc. IEEE 45th Annual International Reliability Physics Symposium (IRPS) (2007) 417-421.

[11] R.W. HERFST, P.G. STEENEKEN, H.G.A. HUIZING and J. SCHMITZ, *Center-shift method for the characterization of dielectric charging in RF MEMS capacitive switches*, IEEE Trans. on Semiconductor Manufacturing **21** (2008) 148-153.

[12] G. PAPAIOANNOU, J. PAPAPOLYMEROU, P. PONS and R. PLANA, *Dielectric charging in radio frequency microelectromechanical system capacitive switches: A study of material PROPERTIES AND DEVICE PERFORMANCE,* Applied Physics Letters **90** (2007).

[14] S. KIM, S. CUNNINGHAM and A. MORRIS, *Characterization of dielectric charging and reliability in capacitive RF MEMS switches*, in Proc. IEEE Int. Reliab. Phys. Symp. (IRPS) (2013) 6B.4.1 - 6B.4.5.

[15] X. ROTTENBERG, I. DE WOLF, B.K.J.C. NAUWELAERS, W. DE RAEDT and H.A.C.

TILLMANS, *Analytical model of the DC actuation of electrostatic MEMS devices with distributed dielectric charging and nonplanar electrodes*, J. of Microelectromech. Syst. 16 (2007) 1243-1253.

[16] M. KOUTSOURELI and G. PAPAIOANNOU, *Determination of long time discharge current in microelectromechanical system capacitive switches*, Appl. Phys. Lett. **99** (2011).

[17] M. KOUTSOURELI, L. MICHALAS, P. MARTINS, E. PAPANDREOU, A. LEULIET, S. BANSROPUN, G. PAPAIOANNOU and A. ZIAEI., *Microel. Reliab.* **53** (2013).

[18] D. BIRMPILIOTIS, P. CZARNECKI, M. KOUTSOURELI, G. PAPAIOANNOU and I. DE WOLF, *Assessment of dielectric charging in capacitive MEMS switches fabricated on Si substrate with thin oxide film*, Microelectronic Engineering **159** *(*2016) 209–214.

[19] HSU H.H. and D. PEROULIS, *A viscoelastic-aware experimentally-derived model for analog RF MEMS varactors*, IEEE 23rd Int. Conf. on Micro Electro Mechanical Systems (MEMS) (2010) 783 – 786.

[20] I. CHASIOTIS, C. BATESON, K. TIMPANO, A.S. MCCARTY, N.S. BARKER and J.R. STANEC, *Strain rate effects on the mechanical behavior of nanocrystalline Au films*, Thin Solid Films, **515** (2007) 3183–3189.

0.13 µm BiCMOS Embedded On-Chip High-Voltage Charge Pump with Stacked BEOL Capacitors for RF-MEMS Applications

M. WIETSTRUCK[1], W. WINKLER[2], A. GÖRITZ[1], S. TOLUNAY-WIPF[1], C. WIPF[1], D. SCHMIDT[1], A. MAI[1], M. KAYNAK[1,3]

[1]IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany
[2]Silicon Radar GmbH, Im Technologiepark 1, 15236 Frankfurt (Oder), Germany
[3]Sabanci University, Orta Mahalle, 34956 Tuzla, Istanbul, Turkey

Abstract. In this paper we demonstrate an on-chip high-voltage charge pump integrated in a 3 µm SiGe:C BiCMOS technology. The charge pump is intended to be used for the actuation of BiCMOS embedded RF-MEMS devices like witches and varactors. A new type of charge pump is introduced using stacked BEOL capacitors as charge/discharge capacitors to overcome the output voltage limitations of charge pumps with standard MIM capacitors. The electrical characterization of both MIM and stacked BEOL capacitor charge pumps show that BEOL capacitors are useful to improve the maximum charge pump output voltage due to extremely reduced leakage currents. By this BiCMOS embedded charge pumps with high output voltages of >60 V can be generated directly on the chip.

Index Terms: RF-MEMS, monolithic integration, BiCMOS, high-voltage charge pump.

1. Introduction

Latest developments in SiGe BiCMOS technologies have shown a tremendous advantage compared to RF-CMOS providing Heterojunction Bipolar Transistors (HBTs) with f_t/f_{max} of 300/500 GHz targeting f_{max} values of 700 GHz [1 – 2]. Beside the high performance HBTs, the existence of a standard CMOS together with advanced technology features like embedded RF-MEMS and Si photonics are key enabling technologies to realize high performance multifunctional mm-wave systems [3].

In recent years a fully embedded RF-MEMS technology module has been developed using the high performance 0.13 µm BiCMOS technologies SG13S/G2. Thanks to these developments monolithic integrated low loss RF-MEMS devices like switches [4] and varactors [5] can be realized directly on the chip. For the actuation of these MEMS devices the electrostatic actuation principle is the preferred solution due to the simple implementation scheme into standard CMOS technologies. Most of the RF-MEMS devices using electrostatic actuation require

high voltages from 40 – 100 V [6 – 7] although low actuation voltage RF-MEMS switches with only 5 V have been demonstrated with the main drawback of large area consumption [8]. Recently we demonstrate two different RF-MEMS devices, a 140 GHz capacitive-type switch [4] and a MEMS varactors [5] with high pull-in voltages of 60–70V in a 0.13 µm BiCMOS embedded RF-MEMS platform.

In the past several on-chip high-voltage charge pumps for MEMS applications have been demonstrated. In [9] a BiCMOS embedded high-voltage charge pump with > 40V output voltages has been demonstrated in a 0.25 µm BiCMOS technology. In [7] and [10] charge pumps with ~50 V output voltage have been realized using a 0.18 µm HV CMOS or 0.6 µm CMOS process respectively. Obviously all these reported charge pump circuits are not suitable due to the limited output voltage if actuation voltages of more than 60 V are required. Beside the consideration of process and design optimization to realize high voltage transistors only minor attention has been given to the influence of charge pump charge/discharge capacitors. Usually only the breakdown voltage has been taken into account as the main criteria for the capacitors. If capacitor breakdown voltages are too low a simple series connection of capacitors can be used to limit the voltage drop for each capacitor. Indeed not only the breakdown voltage has to be considered because capacitor leakage currents can introduce a significant low output resistance limiting the harge pump output voltage. Therefore alternative capacitor types with high breakdown voltages and lowest leakage currents are strongly required to achieve charge pumps with > 60V output voltage for BiCMOS embedded high actuation voltage RF-MEMS applications.

In this paper we demonstrate a high-voltage charge pump integrated in a 0.13 µm SiGe:C BiCMOS technology. A new type of charge/discharge capacitors using stacked BEOL capacitors with lowest leakage current is introduced to overcome the output voltage limitations of charge pumps with standard MIM capacitors.

The electrical characterization of both MIM and stacked BEOL capacitor charge pumps show that stacked BEOL capacitors are very useful to improve the maximum charge pump output voltage for more than 25V due to extremely reduced leakage currents. By this BiCMOS embedded charge pumps with high output voltages of 70V together with high performance RF-MEMS devices become feasible.

2. High-Voltage Generation

A. High-Voltage Generation Circuit

The capacitive charge pump is based on the circuit topology introduced by Pelliconi [11] to provide charge pumps with low power consumption and high efficiency. The main building blocks of a single charge transfer block and the cascaded CP stages are shown in Fig. 1 and a detailed explanation of the circuit operation is provided in [11].

The charge pump is implemented in IHPs 0.13 µm BiCMOS technology SG13G2 including high voltage MOS-transistors and 7 metal layers. Two 24 stage charge pumps were realized to investigate influence of capacitor type. A circuit topology with charging and discharging capability was used to achieve fast operation without requirement of discharge resistors [9].

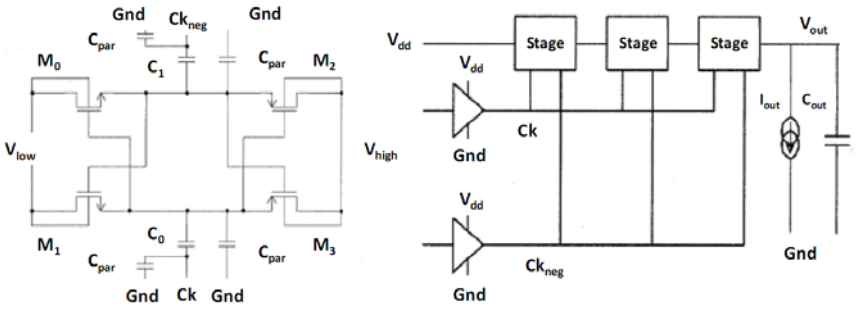


Fig. 1. Main charge pump building blocks: Single charge transfer block (left) and cascaded charge transfer blocks to increase the output voltage [11].

The maximum output voltage is mainly defined by the supply voltage, the capacitors C_0 and C_1 (together with the parasitic capacitances) and the output resistance and output capacitance limiting the maximum achievable output voltage. For the operation of RF-MEMS devices an ideal open-circuit is present thus high output resistances in the GΩ-range are present. But the capacitors itself can introduce a significant low output resistance due to high leakage currents. To analyze the effect of leakage currents on the maximum achievable output voltage charge pumps with standard MIM and stacked BEOL capacitors are fabricated and analyzed.

B. MIM vs. Stacked Metal Capacitors

The two different types of charge/discharge capacitors are analyzed in terms of available capacitance *per area*, leakage current and breakdown voltage. Suitable charge pump capacitors can be realized using either the BEOL MIM capacitors between the Metal-5 (M5) and the TopMetal-1 (TM1) metallization layer with a thin Si_3N_4 dielectric layer or a stacked BEOL capacitor using the parasitic capacitances between the metallization layers with SiO_2 as dielectric layer. In Fig. 2 the cross sections of both capacitor types are shown. MIM capacitors with Si_3N_4 layer as dielectric (ε_r =7) provide a capacitance *per area* of ~1.5 fF/µm². In comparison the stacked BEOL capacitors provide only ~0.3 fF/µm² due to the large SiO_2 thickness ranging from 550–2000 nm in between the different metal layers (ε_r = 4.1) increasing the area to achieve a certain capacitance. Especially for the

stacked BEOL capacitors, additional area is required for the interconnection of the metal layers reducing the effective capacitance *per area*.

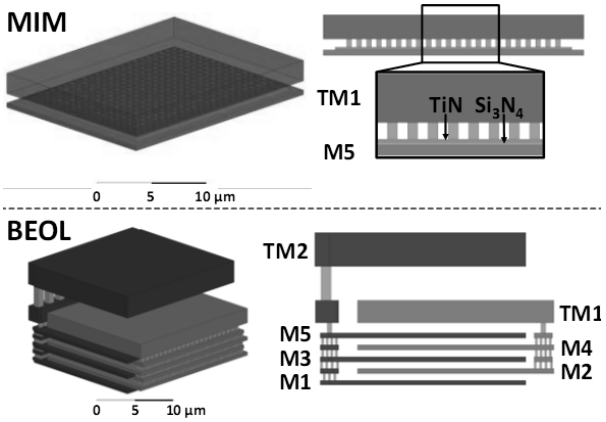


Fig. 2. 3D and cross section view of both MIM capacitor and stacked BEOL capacitor.

Beside the capacitance *per area* the leakage current and the maximum breakdown voltage need to be considered. The leakage current behavior and the breakdown voltage characteristics are analyzed using I-V measurements for fabricated MIM and stacked BEOL capacitor test structures similar to the ones shown in Fig. 3. The voltage is swept between 0–200 V with a current compliance of ~10 µA. I-V measurement results are shown in Fig. 3 for three different chips on a 200 mm wafer.

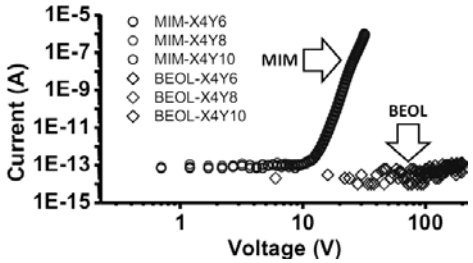


Fig. 3. I-V measurement results for MIM and stacked BEOL capacitor showing a significant difference of the leakage currents.

Obviously there is a significant difference between the MIM capacitor and the stacked BEOL capacitor leakage current. In case of the MIM capacitor, a significant increase of the leakage current can be observed starting from 12 V and reach > 1 µA already at 30V. In comparison the leakage current of the stacked BEOL capacitor is almost constant even up to 200 V with values of < 100 fA.

Based on the I-V characteristics a charge/discharge capacitor lumped element model can be extracted including a parallel capacitor and resistor. Figure 4 shows the equivalent parallel resistance R_{leak} *vs.* the applied voltage. Obviously the resistance R_{leak} is strongly decreasing for the MIM capacitor to values in the MΩ-range. In comparison the R_{leak} is almost constant with values in the TΩ-range for the stacked BEOL capacitor.

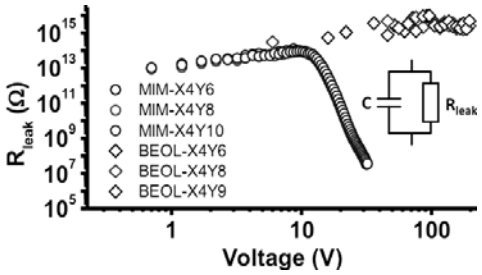


Fig. 4. Leakage current resistor R_{leak} *vs.* applied voltage for MIM and stacked BEOL capacitor extracted from I-V measurements.

Indeed no dielectric breakdown has been observed for the specific MIM and the stacked BEOL capacitors but in case of the MIM capacitor this is related to the current compliance mode limiting the applied voltage. For specific BiCMOS process test structures a MIM breakdown occurs at ~30 V. If charge pumps with more than 60 V output voltages are targeted one MIM capacitor is not suitable to handle these high voltages thus a series connection of at least two MIM capacitors is mandatory.

3. Charge Pump Characterization

For the comparison two types of charge pumps have been fabricated. Microphotographs of the fabricated charge pumps are shown in Fig. 5. The charge pump consumes only ~ 0.2 mm² including the charge transfer blocks, the ring oscillator (RO) and the probe pads.

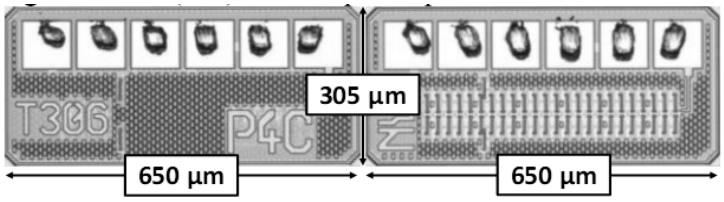


Fig. 5. Microphotograph of the MIM (left) and stacked BEOL capacitor (right) charge pump with dimensions of 650×305 µm².

The input *vs*. output voltage is shown in Fig. 6 for three different chips on the wafer. A fixed ring oscillator control voltage of 3.3 V is chosen. The input voltage is swept from 0–5 V in 200 mV steps. The output voltage is measured using a high measurement input resistance of >10 GΩ. A significant difference between MIM and stacked BEOL capacitor output voltage can be observed. While the MIM capacitor charge pump output voltage saturates already at 40 V with an input voltage of 3.5 V the stacked metal capacitor charge pump can generate output voltages of up to 70 V for a 5 V input voltage.

Beside the output voltage the charge pump current consumption is also measured. In Fig. 7 the overall current consumption of the charge pump including the charge transfer blocks and the RO is shown for different output voltages. Up to 40 V the current consumption of 4 mA is similar for both types of charge pumps. Comparing the achieved output voltage *vs*. the current consumption above 40 V a significant difference between MIM capacitor and stacked metal capacitor charge pump can be observed and an increase of current do not lead to an increased output voltage for the MIM capacitor charge pumps.

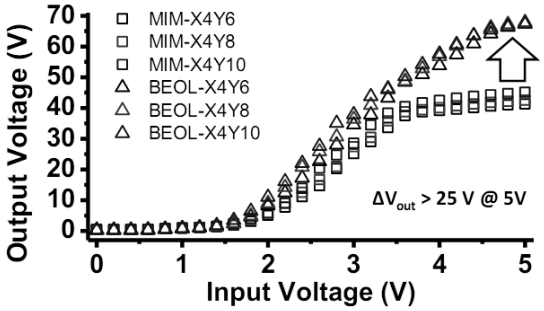


Fig. 6. Output voltage *vs*. input voltage for the MIM and stacked BEOL capacitor charge pumps.

Finally a wafer-level output voltage analysis is done for a fixed input voltage of 5V to compare the uniformity of the charge pump performance on a 200 mm wafer. The wafer-level output voltage is shown in Fig. 8. A significant variation of the maximum output voltage is observed for the charge pumps using MIM capacitors. The reason is the non-uniformity of the Si_3N_4 dielectric layer deposition which can influence the thickness and the leakage current, respectively. For low operation voltages up to 5 V this effect is negligible but for high voltage applications this cannot be ignored. In comparison the output voltage uniformity of the stacked BEOL capacitors is significantly improved with small variations of only 1–2 V. The right side of the wafer has to be excluded due to the position of the charge pumps directly at the right edge of the test chip.

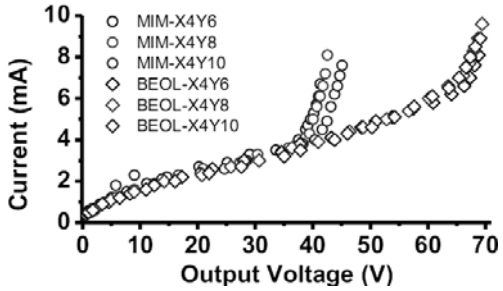


Fig. 7. Current consumption vs. output voltage for the MIM and the stacked BEOL capacitor charge pumps.

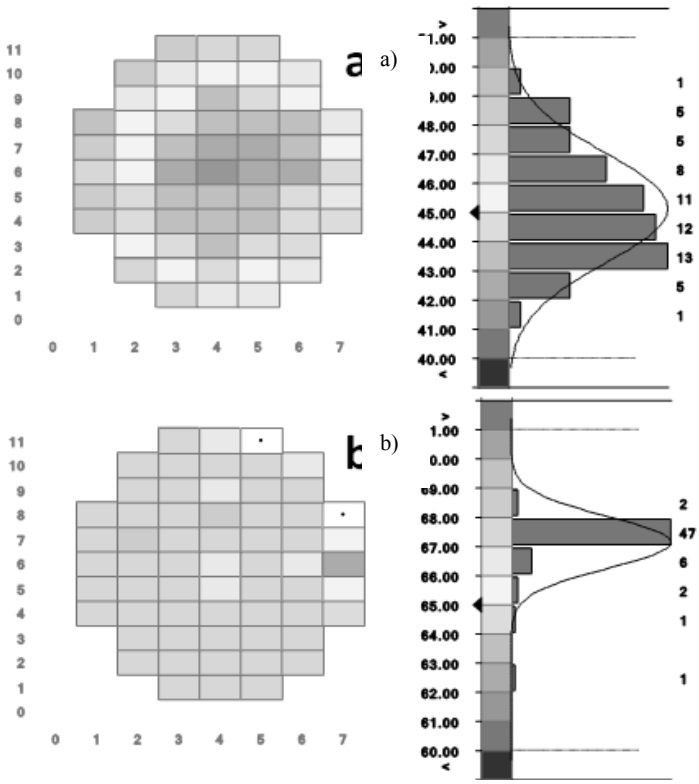


Fig. 8. Wafer-level output voltage for a fixed 5V input voltage for charge pump with a) MIM capacitor and b) stacked BEOL capacitor.

Finally the use of stacked BEOL capacitors for high-voltage charge pumps enables the realization of higher output voltages with an improved uniformity which is an important aspect if sensitive RF-MEMS varactors require very accurate control of the actuation voltages.

4. Charge Pump Reliability Test

Reliability tests are applied to evaluate the long-term reliability of both types of charge pumps. The charge pumps are continuously actuated and the output voltage is measured at every 10 minutes (Fig. 9).

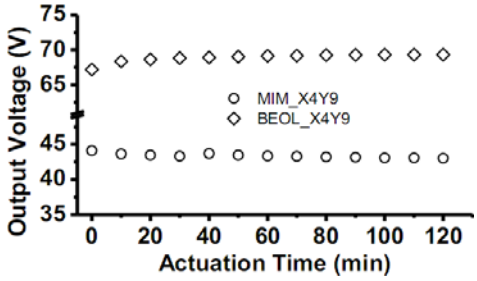


Fig. 9. Measured leakage current *vs*. applied voltage.

No remarkable output voltage variation can be observed. A slight output voltage decrease for the MIM capacitor and a slight increase for the stacked metal capacitor charge pump are observed which can be explained by the charge depletion in the MIM capacitor due to the high leakage current and the charge accumulation in the stacked BEOL capacitors due to the extremely low leakage currents.

5. Conclusion

In this paper we demonstrate a high-voltage charge pump with 70 V output voltage integrated in a 0.13 µm BiCMOS technology. A new type of charge/discharge capacitors using stacked BEOL capacitors with lowest leakage current are introduced to overcome the output voltage limitations of charge pumps with standard MIM capacitors. Stacked BEOL capacitors provide a lower capacitance per area, but due to the negligible leakage current and high breakdown voltages, smaller capacitors can be realized saving area and costs. For the considered technology platform charge pumps with stacked BEOL capacitors are useful to improve the maximum charge pump output voltage of more than 25 V compared to MIM capacitor charge pumps due to extremely reduced leakage currents with very good wafer-level uniformity and reliability.

References

[1] B. HEINEMANN *et al.*, *Advanced Transistor Architectures for Half-Terahertz SiGe HBTs*, ECS Transactions, **50**(9), pp. 61–71, 2012.

[2] http://www.dotseven.eu/, 04.02.2016.

[3] A. MAI *et al.*, *Multifunctional Technology with Monolithic Integrated THz-, Photonic- and µ-Fluidic Modules*, ECS Transactions, **69**(10), pp. 47–54, 2015.

[4] M. KAYNAK *et al.*, *MEMS–BiCMOS Monolithic Integration*, Proc. URSI General Assembly and Scientific Symposium (URSI GASS), 2014.

[5] G. KAHMEN *et al.*, *Static and dynamic characteristics of MEMS Varactor with broad analog capacitive tuning range for wideband RF VCO applications*, European Microwave Conference (EuMC), pp. 1011–1014, 2015.

[6] http://www.radantmems.com/, 04.02.2016

[7] S.P. NATARAJAN *et al*, *CMOS Integrated Digital RF MEMS Capacitors*, 13th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, pp. 173–176, 2011.

[8] A. AKIBA *et al.*, *A fast and low actuation voltage MEMS switch for mm-wave and its integration*, IEEE International Electron Device Meeting (IEDM), pp. 0163–1918, 2010.

[9] M. KAYNAK *et al.*, *A CMOS Based Fast High-Voltage Generation Circuit for BiCMOS Embedded RF-MEMS Applications*, IProc. 13th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2013.

[10] A. EMIRA *et al*, *All-pMOS 50-V Charge Pumps Using Low-Voltage Capacitors*, IEEE Transactions on Industrial Electronicss, **60**(10), pp. 4683–4693, 2012.

[11] R. PELLICONI *et al*, *Power Efficient Charge Pump in Deep Submicron Standard CMOS Technology*, IEEE Journal of Solid-State Circuits, **38(**6), pp. 1068–1071, 2003.

MEMS Varactor Modeling Methodology for interactive Electromechanical Simulation with High Accuracy

GERHARD KAHMEN[1], MATTHIAS WIETSTRUCK[2]
and HERMANN SCHUMACHER[3]

[1]Rohde & Schwarz GmbH, Muehldorfstrasse 15, 81671 Munich, Germany
[2]IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany
[3]Institute of Electron Devices and Circuits, Ulm University, 89069 Ulm, Germany

Abstract. MEMS varactor devices integrated into the *Backend-of-Line* (BEOL) metal stack of a semiconductor process offer an attractive alternative to PN junction or FET gate-channel varactors for monolithic integration of RF-VCOs. Typically the design of MEMS varactors is based on finite element solvers (FEM) and EM field solvers to optimize the electromechanical and RF properties of the devices, which is time consuming and tedious. This paper introduces a methodology for an interactive MEMS varactor design with high accuracy based on a generalized mechanical approach. Additional to the ideal MEMS membrane a composite membrane layer system and the inherent membrane deflection due to residual stress are considered. The good agreement between measurements and predicted results proofs the validity of the presented methodology.

1. Introduction

For frequency tuning of monolithically integrated VCOs, PN junctions or FET gate-channel capacitors are widely used as varactors since most semiconductor processes do not offer dedicated varactor devices. These varactors show significant nonlinearities of the CV characteristic, low RF power handling capability, low tuning voltage range and moderate 1/f noise performance limiting their application to narrow band RF VCOs with moderate phase noise performance. MEMS varactors monolithically integrated into the BEOL metal stack offer an attractive alternative to overcome the above drawbacks [1].

Typically the design of MEMS-varactors is based on finite element (FEM) solvers and electromagnetic (EM) field solvers which is a computationally resource-hungry and time consuming approach. In the literature [2] simple

electromechanical approximations for dedicated topologies can be found which are sufficient to get a general understanding for the MEMS operation, but which cannot be used for an actual MEMS design with given specifications. This paper introduces a modeling methodology based on a generalized electromechanical approach which allows the interactive design of MEMS varactors with high accuracy. As a basis this model considers an ideal single layer planar MEMS membrane. Subsequently the impact of a composite MEMS membrane layer system and an inherent deflection of the MEMS membrane due to residual stress are added. This modeling methodology is demonstrated and verified on a fabricated fixed-fixed MEMS varactor design and can be applied for any kind of MEMS varactor topology.

2. Analytical Calculation of the MEMS Membrane Displacement

The basis for the interactive electromechanical simulation is the analytical calculation of the MEMS membrane displacement *w(x)* when a point force *F* is applied. Figure 1 shows the sectioned model of the MEMS membrane and a photo of the fabricated device.

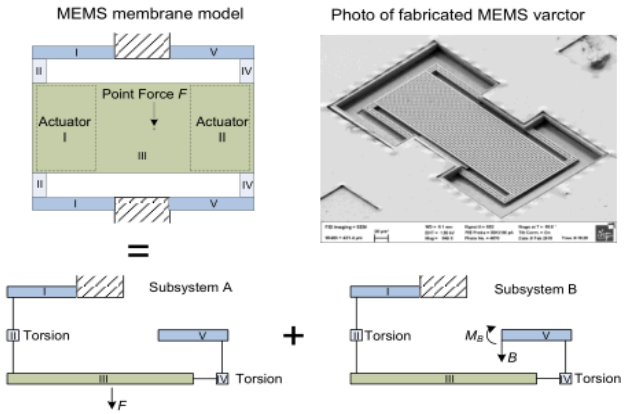


Fig. 1. (Color on line). Model of MEMS membrane and photo of the fabricated MEMS varactor.

The actuators are placed below the MEMS membrane as indicated in Fig. 1. When a force is applied, sections I, V and the MEMS membrane III act as bar springs while sections II and IV act as torsion springs. Since the MEMS membrane as shown in Fig. 1 represents a statically indetermined system it has to be subdivided into two statically determined subsystems with the introduction of the unknown force *B* and moment *MB* as indicated in Fig. 1. In a first step the displacement *w(x,F)* is calculated for subsystem A and *w(x,B, MB)* for subsystem B

making use of the differential equations [3] for the beam displacement with Young's module E, the moment of inertia I, the acting moments M.

$$w'' = -\frac{M}{EI} \tag{1}$$

and the equation for a torsion spring with the shear module G, torsion moment M_T, torsion moment of inertia I_T and length l

$$\vartheta' = \frac{M_T dl}{I_T G} \tag{2}$$

The displacement of the complete membrane is calculated by the superposition of subsystems A and B. The two boundary conditions at the right side of the anchor

$w_A + w_B = 0$ (no displacement at the anchor)
$w'_A + w'_B = 0$ (slope of membrane at anchor is zero)

are applied to calculate the force B and the moment M_B.

3. Electromechanical Simulation of MEMS Membrane Displacement

The electrostatic force which is acting on the MEMS membrane is given by [4]

$$F = \frac{1 \in_0 A}{2d^2} V^2 \tag{3}$$

The MEMS beam represents a linear mechanical system. To consider the distributed geometry of the actuator, the electrodes are subdivided into infinitesimal sub-actuator areas acting as point forces on the MEMS membrane. For each of these point forces the membrane displacement is calculated based on the analytical approach described in section II and then superposed to result in the total displacement of the membrane.

The actual calculation of the displacement, resulting in the equilibrium between the electrostatic force ($F \sim 1/d^2$) and the spring restoring force ($F \sim d$) requires a numerical approach, which is shown in Fig. 2.

Based on the initial gap d_0 and (3) the point forces of the infinitesimal sub-actuators and the resulting superposed displacement of the membrane are calculated giving the updated gap d_1. For this updated gap the infinitesimal point

forces and the new gap d_N are repeatedly calculated again until an equilibrium between electrostatic and restoring force is achieved. This equilibrium is reached if the difference between gap d_n and d_{n+1} is smaller than a predefined error value. Once the equilibrium is reached the capacity of the MEMS varactor is calculated by summing up the infinitesimal capacitor values of the sub-actuator areas applying the parallel plate capacitor equation.

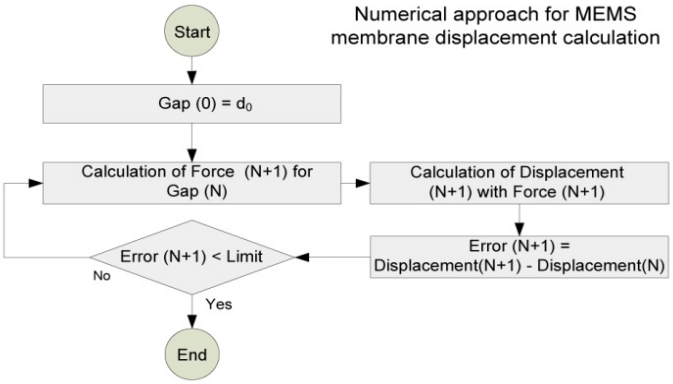


Fig. 2. Numerical approach of the MEMS membrane displacement calculation.

4. Impact of Composite MEMS Membrane Layer

In practice MEMS membranes are realized as multilayer composite systems to compensate the residual layer stress. As an example the MEMS membrane realized within this work is a triple layer TiN-AlCu-TiN stack.

The TiN layers on top and bottom of the AlCu layer are considered by assigning a modified moment of inertia to their cross section applying Steiner's equation [5]

$$I_{\bar{y}} = I_y + \overline{Z}^2 A \tag{4}$$

The modified moment of inertial of the complete composite MEMS membrane is given by with n_{TiN} being the ratio of the Young's moduli of AlCu and TiN.

$$\overline{I} = I_{\bar{y}\mathrm{AlCu}} + n_{\mathrm{TiN}} I_{\bar{y}\mathrm{TiN}} + n_{\mathrm{TiN}} I_{\bar{y}\mathrm{TiN\_u}} \tag{5}$$

The modified stiffness of the composite MEMS membrane is finally given by

$$\overline{EI} = \sum_i E_i I_{\overline{Yi}}^{\ \ \overline{}} = E_{\mathrm{AlCu}}\, \overline{I} \tag{6}$$

5. Impact of Inherent MEMS Membrane Deflection

Residual layer stress within the MEMS membrane can lead to an inherent deflection of the MEMS beam resulting in a significant increase of the MEMS varactors spring constant. Since the practical deflection is small compared to the dimension of the MEMS membrane the triangle approximation shown in Fig. 3 can be applied. The MEMS membrane will be compressed by *2v* in x-direction if a force *F* displaces the membrane by a distance of *u* in z-direction. Due to the law of energy conservation, the spring energy stored in the compressed membrane equals the energy used to displace the membrane by the distance *u* with the applied force F_z.

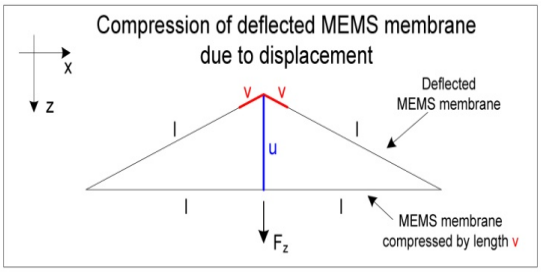


Fig. 3. Compression of deflected MEMS membrane when displaced by a distance *u* and a force *F*.

Equalizing these two energies and applying the law of elasticity results in the spring constant for the compressed MEMS membrane

$$k_S = \frac{F_z}{u} = \frac{EA}{l}\frac{\left(\sqrt{u^2 + l^2} - l^2\right)^2}{u^2} \tag{7}$$

6. Semiconductor Technology

The MEMS varactor developed within this work is embedded in the BEOL metallization stack of the IHP 0.13 µm Si/SiGe BiCMOS technology. This state-of-the-art process offers high speed and high voltage active devices with a BV_{CEO} / f_T combination of 1.7 V / 250 GHz and 3.7 V / 45 GHz, respectively, and a metal

stack of 7 layers. The cross section of the fabricated MEMS varactor is shown in Fig. 4.

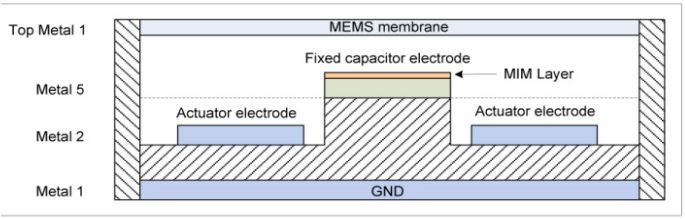


Fig. 4. (Color on line). MEMS varactor configuration within the IHP SG13 BEOL metal stack.

7. Results

Fig. 5 shows measured and simulated CV curves of the realized MEMS varactor. In the varactor CV simulation the effect of the composite MEMS membrane is considered by applying the modified stiffness (6). The inherent deflection due to residual layer stress is accounted for by the additional spring constant (7) acting "in parallel" to the non-deflected ideal MEMS membrane. The simulated pull-in voltage for the ideal single layer AlCu membrane with a Young's module of 70 GPa is 22 V. Taking the triple composite layer stack with ~50 nm and ~100 nm TiN layers (E = 410 Gpa) on top and bottom of the AlCu layer into account results in a pull-in voltage of 32 V.

Adding the effect of the 910 nm inherent membrane deflection due to residual stress leads to an increased distance between the actuators and the MEMS membrane which results in a pull-in voltage of 43 V and a reduced capacitance as expected. The compression of the MEMS membrane due to the deflection in z-direction finally leads to a pull-in voltage of 53 V, which is in good agreement with the CV measurements.

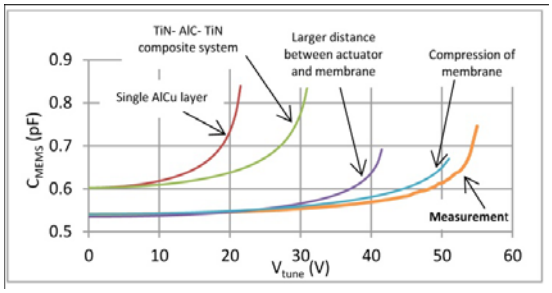


Fig. 5. (Color on line). Measured and simulated CV curves successively including the composite MEMS membrane layer system and the inherent deflection of the membrane.

The time required to simulate each of the CV curves shown in fig. 5 takes less than 20 seconds on a state of the art notebook computer compared to FEM simulations lasting from several minutes to hours depending on the details considered.

8. Conclusion

This work presents an interactive methodology for the electromechanical simulation of MEMS varactors with high accuracy. In addition to the ideal MEMS membrane effects such as a composite membrane layer system and the inherent membrane deflection due to residual stress are considered and can be separated from each other. Due to its high accuracy this methodology can be successfully applied for practical MEMS varactor design and BEOL process optimization.

References

[1] G. KAHMEN, M. KAYNAK, M. WIETSTRUCK, B. TILLACK and H. SCHUMACHER, *MEMS Varactor with High RF Power Handling Capability for Tuning of Wideband Low Noise RF VCOs*, 44th European Microwave Conference, Rome, Oct. 2014, pp. 207 - 210.

[2] G.M. REBEIZ, *RF MEMS: Theory, Design and Technology*, John Wiley & Sons, 2003.

[3] D. GROSS, W. HAUGER, J. SCHROEDER, W.A. WALL, "Engineering Mechanics 2", Springer, 2012, pp. 115 - 118.

[4] H. VOGEL, *Gerthsen Physics*, Springer, 20. edition, p. 306.

[5] D. GROSS, W. Hauger, J. Schroeder, W.A. Wall, *Engineering Mechanics 2*, Springer, 2012, pp. 98 - 99.

Multilayer Micromachining Technology for the Fabrication of Ka Band Filters

B. MARGESIN[1], F. GIACOMOZZI[1], P. FARINELLI[2]

[1]Fondazione Bruno Kessler (FBK), Via Sommarive 18, 38123 Povo Trento, Italy
E-mail: giaco@fbk.eu, margesin@fbk.eu
[2]RF Microtech, Via Mascagni 11, 06132 Perugia, Italy
E-mail: farinelli@rfmicrotech.com

Abstract. This paper presents the manufacturing and testing of a new type of compact and low loss 4th order Ka band filter in multilayer micromachining technology. The filter is based on λ/2 TEM Si membrane resonators placed inside shielding cavities and short-circuited at both anchored ends. The membranes and the cavities are realized by DRIE on SOI wafers and are metalized by gold electroplating. The filter is realized by stacking and bonding six silicon layers for a reduced footprint and area occupation. The RF measurements are very promising, showing insertion loss better than 3dB and Q factors above 500 in Ka-band. Shear tests demonstrated good adhesion of bonded layers and preliminary thermal and mechanical shock test indicated the filter robustness.

1. Introduction

Micromachining technology is one of the most promising alternatives for the realization of high RF performance, low-mass and compact Ka-band filters required for on-board satellite telecommunication [1, 2]. Such a technology allows the realization of metallized cavities and suspended membranes in Silicon or SOI (Silicon On Insulator) substrates. A reduction of device footprint can be obtained with a multilayer approach stacking several cavities by bonding techniques [3, 4].

By properly designing both the input and output planar ports on the same layer it is possible to obtain surface mountable devices that can be easily integrated in standard printed circuits [5].

This paper presents the fabrication technology developed to realize a new type of narrow band 4th order Ka band filter based on the combination of multilayer and micromachining technologies. The filter consists of four resonators placed on

two different levels to reduce the area occupation. Each element is based on a λ/2 TEM membrane resonator suspended inside a shielding cavity and short-circuited to the cavity walls. [6].

The cavities are realized by bonding together two micromachined silicon layers obtained by *Deep Reactive Ion Etching* (DRIE) of SOI wafers. The first one realizes the upper cavity while the second one comprises the 20μm thick silicon membrane and the bottom half of the cavity. All membrane and inner cavity surfaces are metalized by electroplated gold.

The cavities are placed on two levels as schematically reported on Fig 1. Cavities 1–2 as well as cavities 3–4 are coupled vertically while cavities 2–3 and 1–4 are coupled horizontally. A top layer is used as a lid for cavities 1 and 4 and for input and output by depositing on the upper surface microstrip feeding lines that are coupled in resonant mode to the cavities by a thin slot opened in the common ground plane. *Through silicon via's* (TSV) are required for front to back ground connections. The filter design is presented in [7].

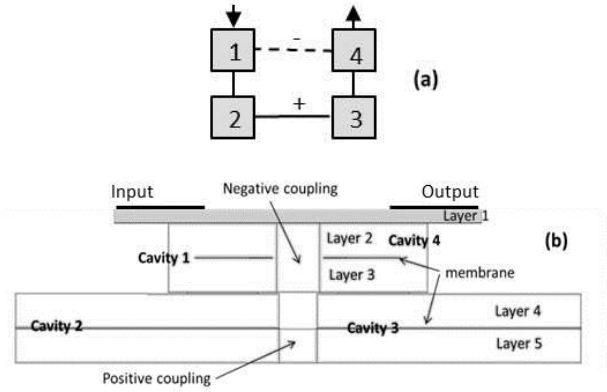


Fig. 1. 4th order Ka band filter topology (a) and schematic cross section (b).

The complete filters are fabricated by stacking six silicon layers: a base layer, four intermediate layers (two layers for each membrane resonator and shielding cavity) and a top layer that provides the RF input and output. A schematic cross section showing the different layers is reported in Fig. 2. The layers are stacked and assembled by gold to gold thermo-compressive bonding, the bonding area is defined by sealing rings realized on the die edges.

Single resonator test structures and two versions of the filter were realized considering surface mounting as well as microstrip to CPW transition to test the devices using probes.

2. Fabrication Process

For the fabrication of the different layers two processes are required: a 6 masks process for the top plate and a 3 mask process for the intermediate layers. The bottom blank layer is obtained by gold plating an oxidized silicon wafer.

In order to reduce the development costs in the first run the chips for intermediate layers were all realized on the same wafer and after dicing the corresponding dies were stacked and assembled by thermo-compression using a flip chip bonder.

The top layer is fabricated on 275 µm thick <100> p type double side polished 5000 Ωcm high resistivity silicon wafers. The fabrication process starts with photolithography and plasma etching to define on the wafer backside the 2 µm thick 50 µm wide sealing rings which define the area for layer to layer bonding at the edge of each device (Fig 3a).

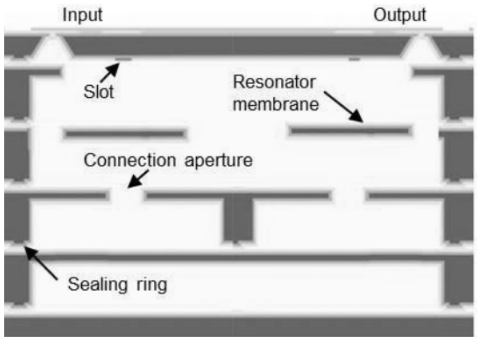


Fig. 2. Schematic cross section of a filter showing the 6 layers.

To realize the hard mask layer on both sides 1 µm thick oxide is grown by steam oxidation at 975°C followed by the deposition of 150 nm thick silicon nitride by LPCVD at 775°C and 300 nm oxide from TEOS at 718°C. The mask for the bottom via's is printed and the dielectric layer dry etched on the wafer backside (Fig 3b). The through silicon via's (TSV), necessary for the front to back ground connection, are obtained by removing the silicon substrate by anisotropic wet etching using *Tetra-Methyl-Ammonium-Hydroxide* (TMAH) to achieve 54.7° angled walls (Fig 3c). The fabrication proceeds by removing selectively the hard-mask layer from the backside of the wafer with a dry etching process to bare silicon leaving the front side exposed membranes nearly untouched because the efficiency of the etching is very low in the narrow holes (less than 50 x 50 μm^2). The exposed silicon surface is steam oxidized to obtain a 1 µm thick oxide to passivate the wafer backside and the TSV walls (Fig 3d). In the next step the TEOS oxide on top of the wafer front side is removed by dry etching and then the silicon nitride is etched by hot phosphoric acid living on the front side only

1μm thermal oxide. The backside of the wafer is coated with a Cr/Au seed layer by PVD and the slots through which the RF signals enters and exit from the cavity are defined. A negative dry film is used because the lamination of the dry film is almost unaffected by the via's holes. The seed layer is wet etched inside the slots and after resist removal a 2.5μm thick gold layer was electro-plated from a cyanide based gold bath to complete the backside processing (Fig 3e).

To provide the electrical connection to the bottom gold layer the top via holes are defined by lithography and the front side oxide membrane dry etched (Fig 3f). A Cr/Au seed layer is deposited on top of the wafers, patterned to define the microstrip input and output RF lines and a 2,5 μm thick gold layer is selectively electroplated. After resist removal the seed layer is wet etched and the gold is annealed at 190 °C for 30 min to improve the adhesion (Fig 3g). To complete the fabrication process the front- side of the wafers is coated with 100 nm thick PECVD oxide layer and the contact holes for the pads are defined and wet etched with buffered oxide etcher (Fig 3h).

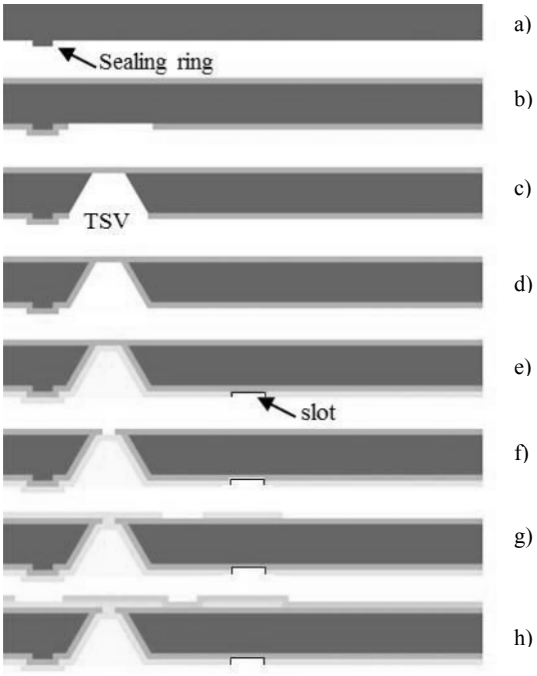


Fig. 3. Processing sequence for the top layer of the Ka band filter.

To fabricate the membranes and the cavities of the intermediate layers DRIE is used to obtain almost vertical sidewalls. The DRIE process is sensitive to the

exposed area and the depth of etching changes from structure to structure and from wafer border to wafer centre. To overcome this potential problem SOI wafers have been chosen as substrate material because the oxide layer between the handle wafer and the top layer can be used as an effective etch-stop for the etch process, allowing an easy and precise control of the membrane thickness within the tolerances of the SOI top layer, typically +/-0.5 μm.

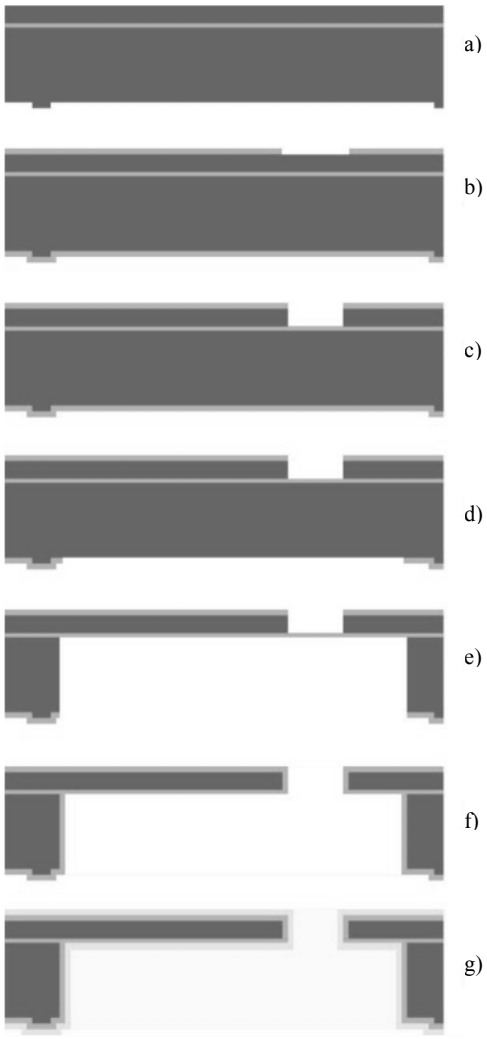


Fig. 4. Processing sequence for the middle layers of the Ka band filter.

The substrates for the intermediate layers process are low resistivity double side polished SOI wafers with a 625 μm thick CZ <100> p type handle wafers, a 1 μm thick buried oxide layer and a 20 μm thick CZ <100> p type device layer. After defining and dry etching the sealing rings on the wafer backside (Fig 4a), a 300 nm thick thermal oxide is grown on both sides by steam oxidation at 975°C. The etch windows for membrane resonators and connection apertures are defined on the wafer front side and the oxide mask dry etched (Fig 4b).

A short DRIE process is used to remove the 20 μm device layer of the SOI up to the buried oxide layer, which acts as an etch stop, and the resist is removed by oxygen plasma (Fig 4c).

A 500 nm thick layer of pure aluminum is deposited by sputtering on the wafer backsides. Next the hard mask for the etching of the bottom cavities is defined by photolithography with thick resist and the aluminum layer and the underneath oxide layer are removed by dry etching (Fig 4d). The cavities are then etched from the backside with a DRIE process for the full depth of the handle wafer by using the buried oxide as an etch stop. (Fig 4e). The residual resist and the passivation polymers on the cavity sidewalls were removed by oxygen plasma and the aluminum layer of the hard mask is removed by wet etching.

After applying an oxygen plasma on both sides, to remove any organic contaminant, the components were stacked starting from the blank bottom plate and adding successively the intermediate layers and the top plate. Each layer was aligned on the previous one with an accuracy in the order of 10 μm and preassembled applying a load of 2 kg (corresponding to a pressure of about 10 MPa) for a few minutes. Once all elements have been stacked correctly the full stack was loaded with 2 kg and heated at 350°C for 45 min by using an interposer plate with the same footprint of the device to apply a uniform pressure on the sealing rings.

The back and front side oxide layers are removed till the bare silicon by dry etching using a high uniformity recipe. Dry etching was chosen in order to avoid the formation of a notch at the level of the buried oxide which would impair the electrical continuity between front and backside of the wafer. After this, a 1 μm thick insulating thermal oxide is grown uniformly on all bare silicon surfaces (Fig 4f) and the wafers are coated with a gold seed layer on both sides. To increase the step coverage on the vertical sidewalls of the cavities, the wafers were mounted at an angle of about 30° with respect to the normal position and two gold deposition were done rotating the wafers of 180° after the first one. To have a uniform metallization a 2.5 μm thick gold film was grown on both sides by electroplating in a fountain plater (Fig 4g). At the end the wafers were annealed at 190°C for 30 min in order to sinter the gold layers.

The wafers were diced by a diamond blade paying attention to not damage the fragile membranes with the water jet of the dicing saw. The dies

corresponding to different layers were selected and assembled by thermo-compression using a flip-chip bond aligner model TRESKY T-3000-FC3.

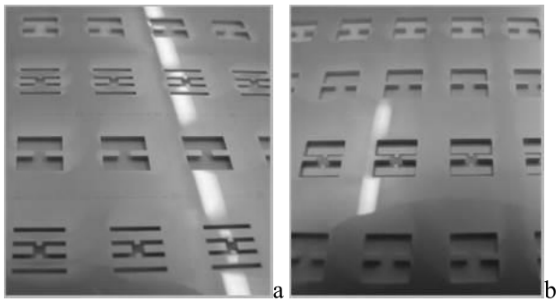


Fig. 5. Presents details of a processed wafer showing some of the intermediate layers dies.

After applying an oxygen plasma on both sides, to remove any organic contaminant, the components were stacked starting from the blank bottom plate and adding successively the intermediate layers and the top plate. Each layer was aligned on the previous one with an accuracy in the order of 10 μm and preassembled applying a load of 2 kg (corresponding to a pressure of about 10 MPa) for a few minutes. Once all elements have been stacked correctly the full stack was loaded with 2 kg and heated at 350°C for 45 min by using an interposer plate with the same footprint of the device to apply a uniform pressure on the sealing rings.

Fig. 6. Pictures of fabricated 4th pole filters.

3. Experimental Results

A few wafers of each kind were processed and diced. Each die was optically inspected and any defective component was discarded. On the top layer a few via's were not completely open while on the intermediate layer a few membranes

were broken during dicing and handling. The majority of the dies were good and about 80 filters could be assembled (Fig 6).

At the end of the fabrication the suspended membrane were almost flat, a slight deflection of just a few micron (2–4) was measured by optical profiler (Fig.7).

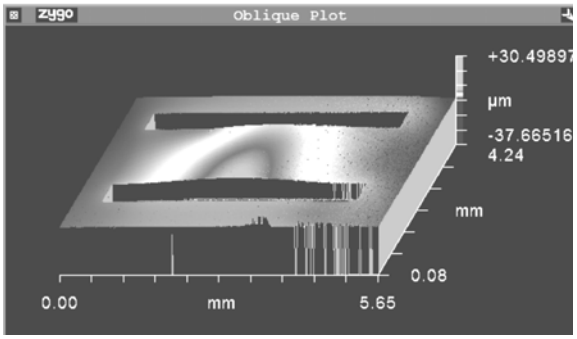


Fig. 7. Optical profiler measurement of a resonator membrane showing a slight deflection of a few microns.

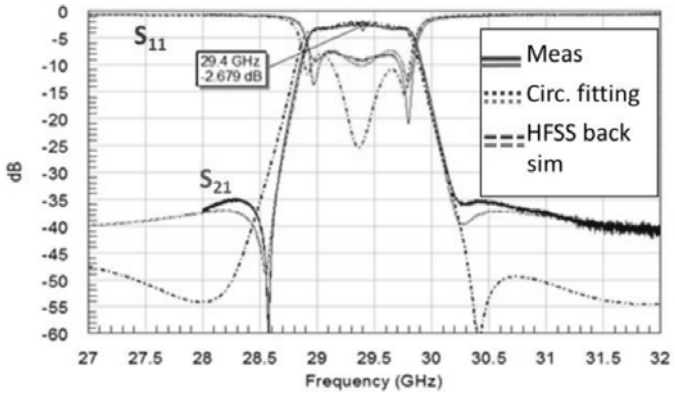


Fig. 8. RF measurements compared with circuital (AWR) and HFSS back simulation, accounting for the actual cavity dimensions.

The filter cavities resulted wider than designed due to not optimal setting of the etching parameters. To reduce nanograss formation, *i.e*. a very rough bottom surface consisting of silicon nanopillars created by the micro- masking effect of polymer residues, the oxygen flow was increased. This reduced the effectiveness of the BOSCH process [8] increasing the removal of protective polymers from the sidewalls and the lateral overetching was much higher than expect, about 60 – 80µm.

Moreover the residual roughness of the bottom surface induced a rough electroplated gold surface.

Figure 8 shows the measured S-parameters of manufactured filter in comparison with circuital and back simulations taking in account the real (measured) cavity dimensions. Due to the longer membranes and larger coupling windows between cavities the resonant frequency down shifted of about 900 MHz respect to the nominal 30 GHz and the return loss was worse than expected. This can be solved in the next fabrication run either by a DRIE process optimization or a cavity mask under sizing.

The filter shows insertion loss below 3dB and a Q factor above 500, slightly lower than predicted very likely due to the high roughness of the cavity bottom interface.

To check the bonding strength shear tests were performed on test samples, which showed that a force of about 4 kg was required to detach the bonded layers indicating good adhesion.

Environmental tests are on-going to demonstrate the space compatibility of the filter. Preliminary tests didn't reveal failures or S-parameters modifications on samples after 10 thermal shock cycles from – 30 °C to 100 °C and after mechanical shocks.

4. Conclusion

A new type of compact and low loss 4th order Ka-band filter was fabricated using a combination of multilayer and micromachining technology.

$\lambda/2$ TEM resonators were realized by metalized silicon membranes placed inside shielding cavities and the cavities are placed on two levels to reduce the footprint.

Through silicon via's on the top level were realized by TMAH anisotropic etching while membranes and cavities were realized by DRIE on SOI wafers and metalized by gold electroplating. The filters were obtained by stacking and gold to gold thermo-compression bonding six silicon layers.

The RF measurements showed insertion loss better than 3dB and Q factors above 500 in Ka-band. The resonant frequency presented a down shift respect to the nominal value due to etching non-idealities that can be solved in the next fabrication run.

Shear tests demonstrated good adhesion of the bonded layers and preliminary thermal and mechanical shock tests indicated the filter robustness.

Acknowledgements. The work has been carried out in the framework of the ESA Project No AO/1-5944/08/NL/GLC. The authors thank Francois Deborgies and Christoph Ernst from ESA/ESTEC for their support and suggestions.

References

[1] L. HARLE, L. KATEHI, *A Silicon Micromachined Four-Pole, Linear Phase Filter*, IEEE Trans. on Microwave Theory and Techniques, **52**(6), 2004.

[2] Y. WANG, M. KE, M.J. LANCASTER, *Micromachined 38 GHz cavity resonator and filter with rectangular-coaxial feed- lines*, IET Microw. Antennas Propag., **3**, pp. 125–129, 2009.

[3] L. HARLE, L. KATEHI, *A vertically integrated Micromachined Filter*, IEEE Trans. on Microwave Theory and Techniques, **50**(9), 2002.

[4] M. STICKEL, P. KREMER, G. V. ELEFTHERIADES, *A Millimeter- Wave Bandpass Waveguide Filter Using a Width-Stacked Silicon Bulk Micromachining Approach*, IEEE Microwave and Wireless Components Letters, **16**(4), 2006.

[5] SANGSUB SONG, CHAN-SEI YOO, KWANG-SEOK SEO, *W- Band Bandpass Filter Using Micromachined Air-Cavity Resonator With Current Probes*, Microwave and Wireless Components Letters, IEEE, **20(**4), pp. 205–207, April 2010.

[6] L. PELLICCIA, P. FARINELLI, R. SORRENTINO, *Micromachined Filters In Multilayer Technology For On-board Communication Systems in Ka-band*, 2013 IEEE MTT-S International Microwave Symposium Digest (IMS), Seattle, 2-7 June 2013.

[7] P. FARINELLI, L. PELLICCIA, BENNO MARGESIN, R. SORRENTINO, *Ka-band Surface-Mountable Pseudo-elliptic Filter in Multilayer Micromachined Technology for On-board Communication Systems*, 2016 IEEE MTT-S International Microwave Symposium Digest (IMS 2016), San Francisco USA, 22-27 May 2016.

[8] S.A. McAULEY, H ASHRAF, L ATABO, A CHAMBERS, S HALL, J HOPKINS and G NICHOLLS, *Silicon micromachining using a high-density plasma source*, J. Phys. D: Appl. Phys. **34**, pp. 2769–74, 2001.

Electrical Properties Of SiN_X Films Doped With CNTs for MEMS Capacitive Switches

M. KOUTSOURELI[a*], G. STAVRINIDIS[b], G. KONSTANTINIDIS[b] and G. PAPAIOANNOU[a]

[a] Physics Department, University of Athens, 15784 Panepistimioupolis, Athens, Greece, Phone: +30 2107276722

[b] Microelectronics Research Group (MRG), IESL-FORTH Hellas, Heraklion, Greece.

*Email: mkoutsoureli@phys.uoa.gr.

Abstract. The present paper aims to provide a better insight on the electrical properties of silicon nitride (SiN*x*) dielectric films with embedded Multi-Walled Carbon Nanotubes (MWCNTs), that can be used in RF MEMS capacitive switches. The effect of the embedded MWCNTs on the leakage current density, on the discharging processes and on dielectric charging phenomena of the films has been probed with the aid of *Metal-Insulator-Metal* (MIM) capacitors

1. Introduction

Capacitive RF MEMS switches are quite promising devices for RF applications, since they offer several advantages over the conventional semiconductor counterparts [1]. They exhibit very attractive performance in terms of linearity, power consumption, losses and isolation. Despite these, MEMS switches suffer from reliability issues [1] that still remain unsolved. One of the most important reliability problem is the effect of dielectric charging, which causes erratic device behaviour and limits the device lifetime [1 – 3].

On the way to solve this problem and prevent dielectric charging phenomena the electrical properties of different dielectric materials [4 – 12] have been intensively investigated. Moreover, several approaches have been proposed up to now, such as the fabrication of MEMS switches with dielectric-dielectric contact [13], the dielectric film removal and replacement with pillars [14] or the

introduction of side actuation pads and the exposure of the CPW capacitor only to RF signal [15]. Despite these, dielectric charging remains an unsolved issue for RF MEMS switches. Meanwhile different theoretical models have been derived that take into account the distribution of injected charges in the insulating film band gap assuming either band tails DOS [16] or a single level of traps [17].

In the case of non-stoichiometric SiN*x* , it has been found that beyond the percolation threshold at $x_c = 1.0$ the Si-Si bonds fail to form continuous percolation paths across the network [18] and thus the Si-rich material has been intensively investigated [4 - 9] in the view of providing a potential solution to mitigate the dielectric charging. An attempt to further increase the percolation paths and therefore the draining of injected charges has been reported by using gold nanorod array structured silicon nitride films [19]. Moreover, the use of carbon nanotubes (CNTs) doped silicon nitride films for RF MEMS switches was presented by C. Bordas *et al* in [20]. This nanostructured dielectric film exhibited a higher *Figure of Merit* [20] that was found to increase with increasing the CNTs density towards the percolation threshold [21]. Finally, the electrical behaviour of multi-walled CNTs (MWCNTs) network embedded in amorphous silicon nitride films of 8 μm thickness has been investigated by Stavarache *et al.*[22], proving the metallic behaviour of the MWCNTs network in silicon nitride matrix.

In view of these, this paper aims to present a different nanostructured dielectric material that consists of silicon nitride with incorporated MWCNTs. The electrical properties of these films have been investigated with the aid of *Metal-Insulator-Metal* (MIM) capacitors by measuring current-voltage (I-V) characteristics and by using *Thermally Stimulated Depolarization Current* (TSDC) and *Kelvin Probe* (KP) assessment methods. A reference SiN*x* material (without MWCNTs) has been also fabricated in order to investigate the impact of the embedded MWCNTs on the leakage current density, on the discharging processes and on the dielectric charging phenomena of the films.

2. Experimental Details

The utilized MIM capacitors (Fig. 1) have been fabricated with symmetric metal contacts (Pt/Au) of 1 mm diameter and the dielectric film was SiN*x* with embedded MWCNTs. The dielectric film has been fabricated with the following steps: First, 100 nm SiN*x* has been deposited on the bottom electrode with PECVD method. After that a solution of MWCNTs with propanol was deposited via spin coating and then a final layer of 100 nm SiN*x* was grown by PECVD to embed the MWCNTs. We mention that the diameter of the MWCNTs used in the present work is 1 nm and their length is 2 – 3 μm. Apart from these, a reference sample with SiN*x* has been fabricated by PECVD method in two steps (100 nm each step)

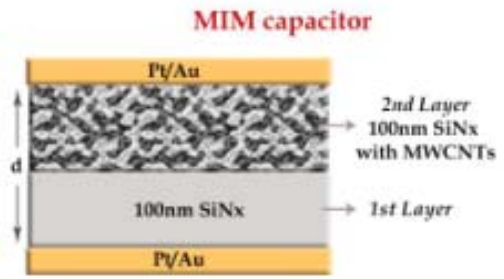


Fig. 1. Schematic representation of utilized MIM capacitors.

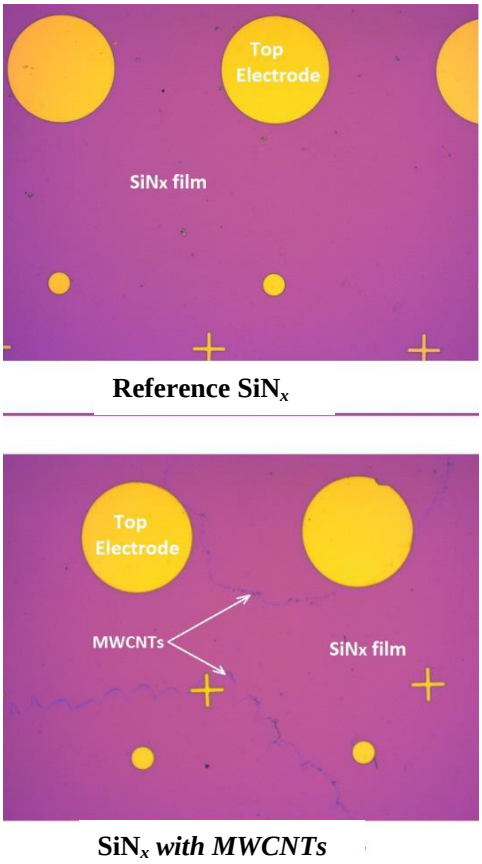


Fig. 2. (Color on line). Photos of utilized samples with reference SiNx films (top) and SiNx films with embedded MWCNTs (bottom). White arrows show the embedded MWCNTs.

without using MWCNTs solution. Fig. 2 shows a photo of utilized MIM capacitors with reference SiN_x films and with SiN_x films doped with MWCNTs.

The capacitance of the samples has been measured with the aid of a Boonton 72B capacitance meter with a resolution of 0.05 fF.

Current-voltage (I-V) characteristics have been obtained for fields up to 2 MV/cm with the aid of a Keithley 6487 source-meter/electrometer. The DC bias was applied to the top electrode and the voltage ramp on I-V measurement was performed with a rate of 100 mV/s. We also mention that I-V measurements were performed in a vacuum cryostat and at room temperature.

The MIM capacitors have been also assessed with Thermally Stimulated Depolarization Currents (TSDC) technique in order to investigate dielectric charging phenomena. The polarization field's intensity was 2 MV/cm and the polarization bias has been applied to the top electrode of MIM capacitors at 450 K. The TSDC current has been measured under vacuum with the aid of a Keithley 6487 voltage source – picoampere meter, in the temperature range of 200 – 450 K and with a heating rate of 2.5 K/min.

Finally, the discharging process through the bulk material has been investigated with the aid of a single-point Kelvin Probe system (KP010), at room temperature and at ambient conditions. The Kelvin Probe is a non - contact, non-destructive vibrating capacitor device used to measure contact potential difference between a conducting specimen and a vibrating probe tip which is placed near the surface of interest. The surface potential of the utilized devices is thus directly measured during discharge, while the device is not in contact with the measuring system. A polarization field with intensity 1 MV/cm and 2 MV/cm has been applied for 5 min at room temperature. The following discharging process has been assessed by measuring the decay of surface potential using a Single Point Kelvin Probe system (KP010) for a time period of about 10^4s.

4. Results and Discussion

The capacitance of the utilized samples has been found to increase about 2% when MWCNTs are embedded into SiN_x matrix.

Figure 3 shows the I-V characteristics of MIM capacitors with reference SiN_x material and with SiN_x material doped with MWCNTs. It is thus interesting to notice that the leakage current of SiN_x/MWCNTs films is quite larger (*i.e.* almost two orders of magnitude) than the reference material.

In order to understand this behavior, it is important to bear in mind the following: The length of the incorporated MWCNTs is quite larger than the thickness of the second SiN_x layer (100 nm) and so it is expected that the MWCNTs will be distributed along the second SiN_x layer, thus producing an inhomogeneous electric field across this layer. Taking these into account and

neglecting any interfacial phenomena that may be present between the two SiN_x layers (due to the step deposition process of the SiN_x material), we expect that when we apply a potential difference V across the metal electrodes of the MIM capacitor the applied electric field on the reference material will be homogeneous and its intensity will be V/d (d is the thickness of SiN_x film). On the contrary, the applied electric field across the SiN_x film with MWCNTs is expected to be inhomogeneous and its intensity is expected to vary between V/d and $2V/d$, since

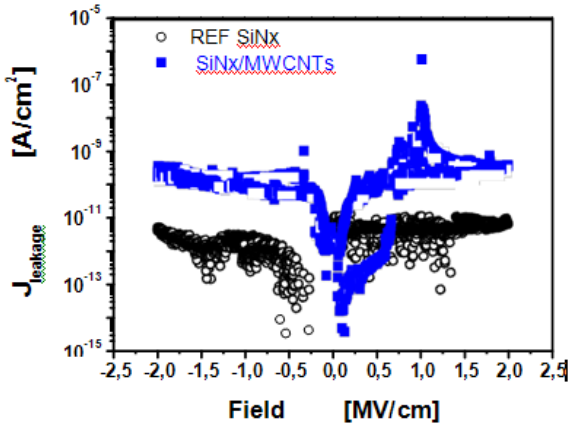


Fig. 3. I-V characteristics for reference SiN_x material and SiNx with embedded MWCNTs.

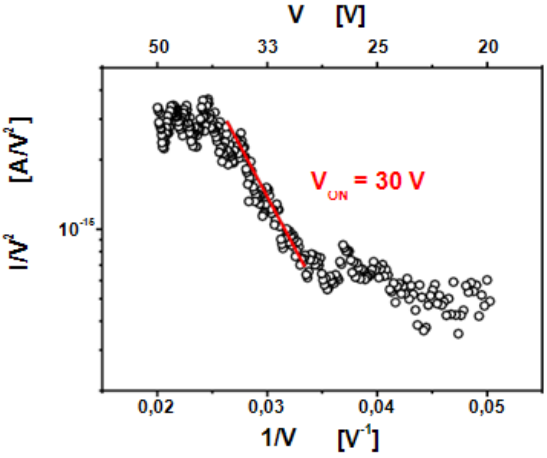


Fig. 4. FN signature plot for SiN_x with embedded MWCNTs films, in agreement to Eq. 1.

it is possible that some MWCNTs may extend across the second SiNx layer up to

the top electrode.

Apart from these, I-V characteristics revealed that field emission processes between CNTs arise on SiN_x films when MWCNTs are present, for applied electric field intensities larger than 1.5 MV/cm. Figure 4 presents the characteristic signature plot of *Fowler-Nordheim* (FN) mechanism that describes field emission processes. *Fowler–Nordheim* (FN) theory describes the emission of electrons from a metal due to very high electric field and it takes place through sharp asperity paths, where the electric field is locally enhanced by several orders of magnitude. In terms of measured current (I) *versus* applied bias (*V*) the Fowler–Nordheim equation is expressed as [23]:

$$I = A \cdot V^2 \cdot \exp\left(-\frac{B}{V}\right), \tag{1}$$

where A is a parameter proportional to effective emitting area (α) and the parameter B is inversely proportional to field enhancement factor (β) [23]. Assuming that the work function of the MWCNTs in our case is $\Phi = 4.5$ eV [24] we thus obtain that the effective emitting area is $\alpha = 4.3 \times 10^{-20} cm^2$ and the field enhancement factor is found to be $\beta = 2.2 \times 10^6$ cm^{-1}. We mention that field emission has been also found to dominate conductivity on CNTs filled Polydimethylsiloxane composites [25].

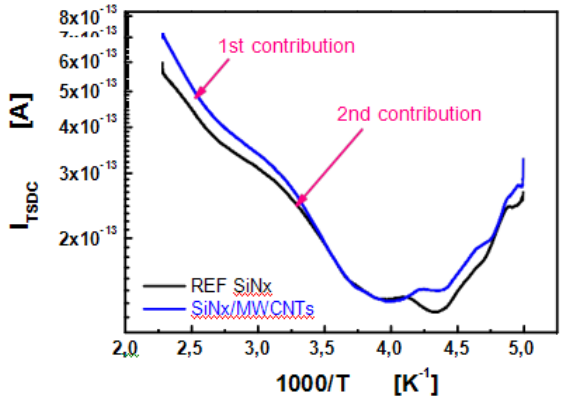


Fig. 5. TSDC spectra for reference SiN_x material and SiN_x with embedded MWCNTs.

TSDC assessment revealed that there is a minimum number of two contributing charging mechanisms on SiN_x films (Fig. 5) that have been

measured. Moreover, dielectric charging is enhanced when MWCNTs are incorporated in the SiN_x matrix. This may be attributed to the fact that the

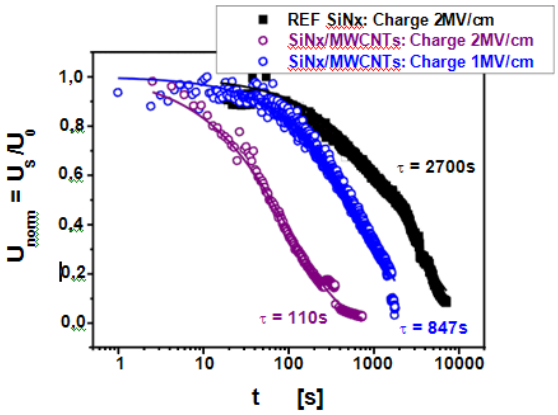


Fig. 6. Normalized values for the surface potential decay during discharge measured with KP system, for reference SiN_x material and SiN_x with embedded MWCNTs after charging the films for 5 min with electric field intensities of 1 MV/cm and 2 MV/cm.

polarization field intensity on SiN_x/MWCNTs films is expected to be inhomogeneous and with larger intensity than the corresponding values that apply on the reference SiN_x material, as mentioned previously.

Field emission processes that arise on SiN_x/MWCNTs films may also be responsible for enhanced dielectric charging phenomena on these films.

Finally, the discharging process through the bulk material has been investigated with the aid of KP method. The decay of surface potential (U_S) has been found to obey a stretched exponential law of the form:

$$U_s(t) = U_0 \cdot \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right], \qquad (2)$$

where U_0 is the surface potential immediately after charging (*i.e.* at t = 0 s), τ is the characteristic time of the discharging process and β is the stretched exponential factor with $0 < \beta < 1$. As presented on Fig. 6, it has been found that the incorporation of MWCNTs results to a decrease of the relaxation time to almost one order of magnitude. Further decrease of the discharging relaxation time has been observed on SiN_X/MWCNTs films as the intensity of the polarization field increases (Fig. 6). The increase of polarization field intensity is

expected to shiftthe injected charges centroid deeper inside the film and thus facilitating charge collection from the bottom electrode.

6. Conclusion

A nanostructured dielectric material for RF MEMS capacitive switches has been fabricated by doping PECVD SiN_X films with MWCNTs. The fabrication process is quite simple and it takes place in two steps, in order to incorporate MWCNTs on the upper SiN_X layer. The electrical conduction processes of these films have been probed with the aid of MIM capacitors by measuring I-V characteristics and dielectric charging phenomena have been investigated with the aid of TSDC method. It has been then found that films with embedded MWCNTs exhibit larger leakage current density and field emission processes arise on these films when the intensity of the polarization field becomes larger than 1.5 MV/cm. The capacitance of the samples has been found to increase about 2% when MWCNTs are incorporated into SiN_X matrix and dielectric charging is also enhanced on SiN_X/MWCNTs films. Finally, the discharging process due to charge displacement through the bulk material and towards the bottom electrode has been probed with the aid of a Kelvin Probe single-point system and it has been found to be accelerated when MWCNTs are embedded into SiN_X material.

Acknowledgements. The first author, Matroni Koutsoureli, would like to thank "IKY Fellowships of Excellence for Postgraduate Studies in Greece – Siemens Program" that takes place in the framework of the Hellenic Republic – Siemens Settlement Agreement.

References

[1] G.M. REBEIZ, *RF MEMS, Theory, Design and Technology*, Hoboken, Wiley, New Jersey, USA, 2003.

[2] W.M. VAN SPENGEN, R. PUERS, R. MERTENS, I. DE WOLF, *A comprehensive model to predict the charging and reliability of capacitive RF MEMS switches*, J. Micromech. Microeng. **14**, pp. 514-521 (2004).

[3] X. ROTTENBERG, I. DE WOLF, B.K.J.C. NAUWELAERS, W. DE RAEDT, H.A.C. Tillmans, *Analytical model of the DC actuation of electrostatic MEMS devices with distributed dielectric charging and nonplanar electrodes*, J. of Microelectromech. Syst. **16**, pp. 1243-1253 (2007)

[4] M. KOUTSOURELI, N. TAVASSOLIAN, G. PAPAIOANNOU and J.PAPAPOLYMEROU, *Dielectric charging in capacitive microelectromechanical system switches with silicon nitride,* Appl. Phys. Lett. **98**, 093505 (2011).

[5] M. KOUTSOURELI, E. PAPANDREOU, L. MICHALAS and G. PAPAIOANNOU, *Investigation of silicon nitride charging*, Microel. Engineering **90**, pp. 145–148 (2012).

[6] M. LAMHAMDI, P. PONS, U. ZAGHLOUL, L. BOUDOU, F. COCCETTI, J. GUASTAVINO, Y. SEGUI, G. PAPAIOANNOU and R. PLANA, *Voltage and temperature effect on dielectric charging for RF-MEMS capacitive switches reliability investigation*, Microel. Reliability **48**, pp. 1248-1252 (2008).

[7] R.DAIGLER, E. PAPANDREOU, M. KOUTSOURELI, G. PAPAIOANNOU and J. PAPAPOLYMEROU, *Effect of deposition conditions on charging processes in SiNx: Application to RF-MEMS capacitive switches*, Microel. Engineering **86**, pp. 404–407 (2009).

[8] U. ZAGHLOUL, G. PAPAIOANNOU, F. COCCETTI, P. PONS and R. PLANA, *Dielectric charging in silicon nitride films for MEMS capacitive switches: Effect of film thickness and deposition conditions*, Microel. Reliability **49**, pp. 1309-1314 (2009).

[9] N. TAVASSOLIAN, M. KOUTSOURELI, G. PAPAIOANNOU and J. PAPAPOLYMEROU, *Optimization of dielectric material stoichiometry for high-reliability capacitive MEMS switches*, IEEE Microwave and Wireless Components Lett. **26** (3), pp. 174-176 (2016).

[10] C.L. GOLDSMITH and D.I. FOREHAND, *Temperature variation of actuation voltage in capacitive MEMS switches*, Proc. IEEE Microwave and Wireless Comp. Lett. **15** (10), 718-720 (2005).

[11] C.F. HERRMANN, F.W. DEL RIO, D.C. MILLER, S.M. GEORGE, V.M. BRIGHT, J.L. EBEL, R.E. STRAWSER, R. CORTEZ and K.D. LEEDY, *Alternative dielectric films for rf mems capacitive switches deposited using atomic layer deposited Al2O3/ZnO alloys*, Sens. Actuators A, Phys. **135** (1) 262–272 (2007).

[12] A. PERSANO, F. QUARANTA, A. COLA, M.C. MARTUCCI, P. CRETI, A. TAURINO, P. SICILIANO, R. MARCELLI, G. DE ANGELIS and A. LUCIBELLO, *Alternative materials for RF MEMS switches in III-V technology*, Proc. IEEE Symp. on Design Test Integration and Packaging of MEMS/MOEMS (DTIP), pp. 295–298 (2010).

[13] D. MOLINERO , S. CUNNINGHAM, D. DE REUS AND A. MORRIS, *Dielectric charging characterization in MEMS switches with insulator-insulator contact*, Proc. IEEE Int. Reliab. Phys. Symp. (IRPS), 5C.3.1 - 5C.3.4 (2014).

[14] V. MULLONI, F. SOLAZZI, G. RESTA, F. GIACOMOZZI and B. MARGESIN, *RF-MEMS switch design optimization for long-term reliability*, Analog Int. Circ. and Signal Proc. **78** (2), pp. 323-332 (2014).

[15] K. SANGCHAE, J. MC KILLOP and A. MORRIS, *Characterization of dielectric charging and reliability in capacitive RF MEMS switches*, Proc. IEEE Int. Reliab. Phys. Symp. (IRPS), 6B.4.1-6B.4.5 (2013).

[16] G. PAPAIOANNOU, F. COCCETTI and R. PLANA, *On the modelling of dielectric charging in RF-MEMS capacitive switches*, Proc. IEEE Topical Meeting on Silicon Monolithic Integr. Circ. in RF Systems (SiRF), pp. 108-110 (2010).

[17] A. JAIN, S. PALIT and M.A. ALAM, *A physics-based predictive modeling framework for dielectric charging and creep in RF MEMS capacitive switches and varactors*, J. of Microelectromech. Syst. **21**, 420-430 (2012).

[18] J. ROBERTSON J., *Electronic structure of silicon nitride*, Philosoph. Magazine **63**, pp. 47-77 (1991).

[19] L. MICHALAS, S. XAVIER, M. KOUTSOURELI, O.E. JOUAIDIS, S. BANSROPUN, G. PAPAIOANNOU and A. ZIAEI, *Gold nanorod array structured silicon nitride films for reliable RF MEMS capacitive switches*, Proc. IEEE Topical Meeting on Silicon Monolithic Integr. Circ. in RF Systems (SiRF), pp. 89-91 (2015).

[20] C. BORDAS, K. GRENIER, D. DUBUC, E. FLAHAUT, S. PACCHINI, M. PAILLARD and J.L. CAZAUX, *Carbon Nanotube based dielectric for enhanced RF MEMS reliability*, Proc. IEEE MTT-S Int. Microwave Symp., pp. 375-378 (2007).

[21] F. DU, J.E. FISCHER and K.I. WINEY, *Effect of nanotube alignment on percolation conductivity in carbon nanotube/polymer composites*, Phys. Rev. B **72**, 121-404 (2005).

[22] I. STAVARACHE, A.M. LEPADATU, V.S. THEODORESCU, M.L. CIUREA, V. IANCU, M. DRAGONMAN, G. KONSTANTINIDIS and R. BUICULESCU, *Electrical behaviour of multi-walled carbon nanotube network embedded in amorphous silicon nitride*, Nanoscale Research Lett. **6:8**, 1-6 (2011).

[23] R. H. FOWLER and L. NORDHEIM, *Electron emission in intense electric fields*, Proc. of the Royal Soc. of London. Series A, Containing Papers of a Mathematical and Physical Character **119**, 173–181 (1928).

[24] W.S. SU, T.C. LEUNG and C.T. CHAN, *Work function of single-walled and multiwalled CNTs: First principles study,* Phys. Review *B* **76**, 235413 (2007).

[25] P. MIMIGIANNI, F. GIANNAKOPOULOU, G. TSIAKATOURAS, M. KOUTSOURELI, G. PAPAIOANNOU and S. NITODAS, *Conduction mechanisms in conductive multi-walled carbon nanotube filled polydimethylsiloxane nanocomposites*, Microel. Engineer. **159**, 198-201 (2016).

Widely Tunable MEMS LC Tank for Multi–Band Applications

A. CAZZORLA[1], P. FARINELLI[1], F. GIACOMOZZI[2], R. SORRENTINO[3]

[1]RF Microtech, via Mascagni 11, 06132 Perugia, Italy
[2]Fondazione Bruno Kessler FBK, Via Sommarive 18, I–38123 Povo Trento, Italy
[3]University of Perugia, Perugia, Italy

Abstract. This paper presents the modeling and simulations of compact multi-band MEMS based LC tank resonator suitable for very low phase-noise VCO. The resonator is based on a high-Q spiral inductor and high capacitive ratio varicap fully integrated in FBK-irst MEMS manufacturing process. The design of the varicap is based on double actuation mechanism with a mechanical central bond that inhibits the pull-in allowing for a theoretically infinite tuning ratio. The measurements show a total *Capacitance ratio* (Cr) of 5.2 with two continuous tuning range with a Cr* = 1.6 and 2.6. The spiral inductor consists of a suspended gold membrane thick 5μm in circular shape. The simulations show that the MEMS based resonator allows for an overall tuning range of 60% in the frequency range 2.15 - 3.85GHz. Two separate regions of continuous tuning range (9.5% and 30%) allow one to cover the whole frequency spectrum of WiMAX and IEEE802.11a/b/g/n. The simulated quality factor (Q) is about 60. A preliminary design of the MEMS based *Voltage Controlled Oscillator* (VCO) was performed using *Advanced Design System* (ADS®). Bonding wire interconnections have been also considered and optimized for improved performance. The VCO prototype is being fabricated on *Surface Mount Technology* (SMT) on RO4350 laminate.

Key words: MEMS; Quality Factor; Spiral Inductor; VCO; Varactor;

1. Introduction

With the recent developments in the wireless communication industry, the demands for radios covering the whole frequency spectrum of fixed and mobile WiMAX, and IEEE 802.11a/b/g/n is desired together with minimum hardware resources and costs [1, 2]. In many RF transceiver systems, the voltage controlled oscillators (VCO) are key components since they are the source of the reference oscillation frequency. In conventional harmonic VCO, oscillation frequency is basically determined by the resonant circuit (typically an LC circuit called LC

tank) and the frequency tuning can be achieved by varying the voltage dependent capacitance of the varicap element in the LC tank. Low phase noise and wide tuning range are the main requirements, imposed by the market, for the design of a VCO to be used in new generation front-end circuits.

As reported in literature [3], the phase noise of a VCO depends on many factors like oscillator output power, output oscillation frequency, operating temperature and quality factor (Q) of the LC resonant circuit. The latter is considerably limited by the losses of the passive elements, such as on-chip spiral inductors [4], as well as substrate and conductor losses. In addition, the use of on-chip spiral inductors is limited in frequency by their *self-resonance frequency* (SRF). At this frequency, the coupling capacitance between inductor eddy current and the substrate forms a parallel resonance [5]. It represents a limiting factor if high inductance values are required. In conventional CMOS fabrication process, much effort has been devoted to the enhancement of inductor performance in terms of Q-factor and self-resonance frequency, as reported in [6, 7]. An alternative to conventional CMOS fabrication process is represented by the micro-electromechanical (MEMS) technology [8] which allows to achieve highly miniaturized LC resonators with high-Q performance.

This paper presents a compact multi-band MEMS LC series resonator based on a spiral inductor and a varicap, fully integrated in MEMS manufacturing process. The MEMS based LC tank allows one to design a VCO that can simultaneously operate in the IEEE 802.11b/g (WLAN) and IEEE 802.16d (WiMAX) standards. Measurement results of the MEMS varicap together with mechanical and electromagnetic analyses of high–Q MEMS spiral inductor are presented. Finally, the modeling of the MEMS based LC tank, accounting for bonding wires interconnection, is shown and the simulation results are compared with the state of the art.

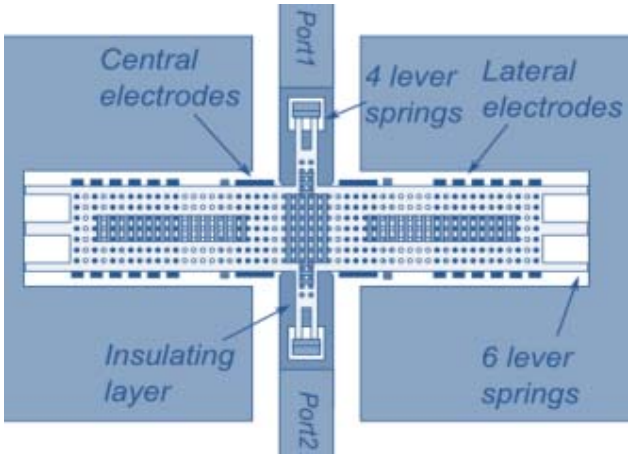
2. Resonator Design

A. MEMS Varicap

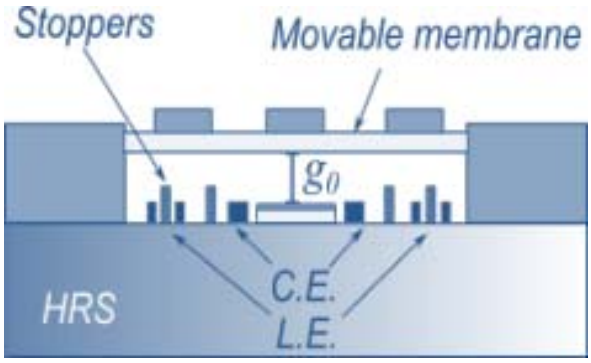
Figure 1 shows the layout and cross–section of the MEMS varactor to be used in the LC tank.

The device consists of a movable membrane placed in shunt configuration with respect to a *coplanar waveguide* (CPW) RF line, on *high resistivity silicon* (HRS) substrate, 625 μm thick. The device is based on a double actuation this purpose, the DC electrodes have been split into two separate electrodes, called L.E. (*lateral electrodes*) and CE (*central electrodes*) as shown in Fig. 1a [9]. When no voltage is applied, the residual gap g_0 is 2.5 μm, (Fig. 1b) and the device shows a measured capacitance of 115 fF. By applying an increasing DC control voltage

from 0 V up to 35 V on the L.E., the capacitance continuously increases up to 185fF, corresponding to a capacitive ratio of about 1.6. For voltages higher than 40



a)



b)

Fig. 1. MEMS Varicap: a) Top view; b) Cross section.

V, the bridge snaps down. However, the complete membrane snap-down above the RF line is avoided thanks to the 4 lever springs in the central part of movable membrane. In this state, the device shows a capacitance of 225 fF. Then, by applying a DC signal from 0 V to 60 V on the C.E., the residual gap is continuously decreased allowing for a further continuous tuning (capacitive ratio (Cr*) of 2.6 corresponding to a measured capacitance of 600 fF). To sum, the varicap presents two regions of continuous tuning providing an overall capacitive ratio (Cr) of 5.2, Fig. 2.

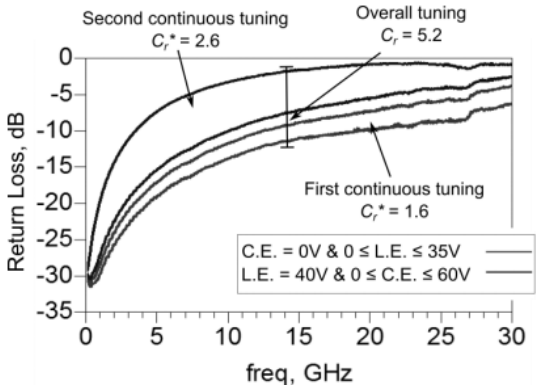


Fig. 2. MEMS Varicap: measured return loss as function of the applied voltage. Cr* and Cr stand for continuous and non-continuous capacitive ratio.

B. MEMS Spiral Inductor

The proposed spiral inductor is shown in Fig. 3a. It consists of a 5 μm thick gold suspended membrane in circular shape of external diameter D_{ext} of about 440 μm. D_{int} is the internal diameter of the structure. S and w are the spacing among turns and the width of the wire conductor, respectively. The spiral inductor was designed to be manufactured in FBK-irst MEMS process [10], monolithically integrated with the MEMS varicap described above.

Since the suspended structure (Fig. 3b, $g_0 \approx 2.7$ μm) is sensitive to process stresses, a mechanical analysis was performed in ANSYS® multiphysics environment in order to simulate the residual stress condition. For the Young modulus (E), the residual stress (σ) and gradient of stress σ(z) of the gold membrane, the values of 75 GPa, 60 MPa and 12 MPa were used. Fig. 4a shows the delta displacement (Δ – z) along z axis, just after the release of the structure. The suspended conductor is up–warped of + 0.1 μm and down–warped of – 6 μm, resulting in an unpredictable inductance value, since the coupling capacitance between spirals is abruptly changed. In order to ensure high conductor flatness, mechanical pillars, equally spaced at the distance of about 60μm, were inserted in the design. Resulting delta displacement (Δ–z) along z axis , just after the release of the structure, is shown in Fig. 4b. 15μm × 15μm square pillars are fabricated below the suspended inductor without changing the manufacturing process.

Afterwards, the device was designed in CPW technology and was simulated in ANSYS® HFSS full–wave environment in the 0 – 30 GHz frequency range. HRS substrate, 625 μm thick, was used. The main responsible of the low-Q performance was found to be the thinner metal below suspended conductor, named underpass in Fig. 3b. As consequence, in order to maximize the quality factor (Q)

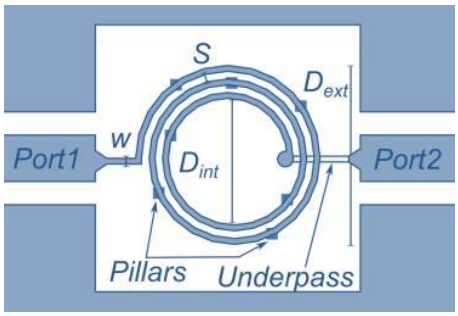


Fig. 3. MEMS spiral inductor: a) Top view; b) Cross section.

and the *self-resonance frequency* (SRF) of the device, two different solutions were implemented: the first one was to increase the thickness of the underpass metal, from the standard value of 0.6μm up to 1.2 μm reducing the conductor loss due to the skin effect. The second one was to partially remove the silicon substrate reducing the substrate loss and the parasitic coupling with the inductor. *Deep reactive-ion etching* (DRIE) will be used to create deep penetration with high aspect ratio in the substrate.

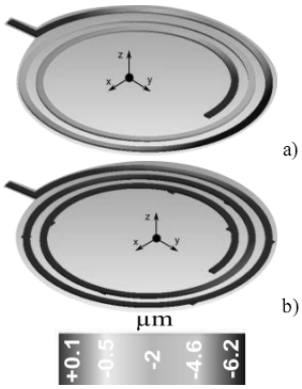
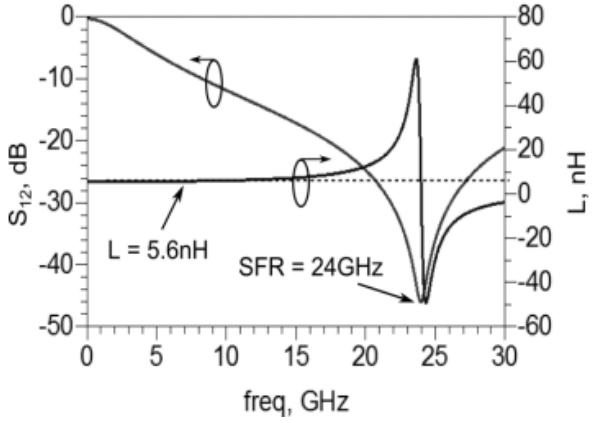


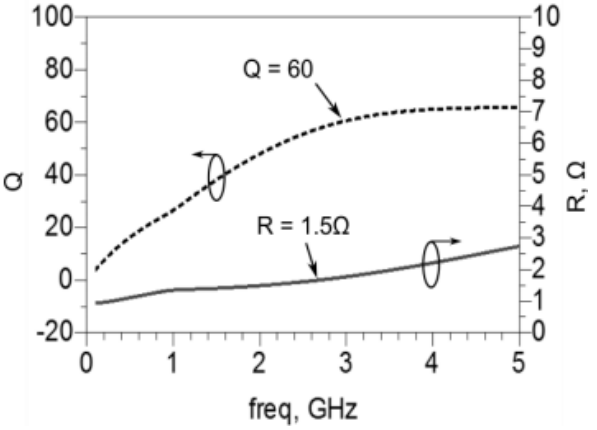
Fig. 4. Delta displacement just after the release of the structure: a) without pillars; b) with pillars.

Simulated S-parameters and inductance (L) are shown in Fig. 5a. In Fig. 5b, the simulated equivalent series resistance (R) and the quality factor (Q) are reported.

Up to 10 GHz, the device exhibits a theoretical inductance of about 5.6 nH. Very high self-resonance frequency (SRF) of about 24 GHz is achieved thanks to the fact that the conductor is suspended. Up to 5 GHz, the resistance is in the range 1Ω – 2.7 Ω, resulting in a Q higher than 60 at 3 GHz.



a)



b)

Fig. 5. HFSS simulation results: a) S12, L and b) R, Q for the proposed MEMS spiral inductor.

By using the equivalent π-model circuit, the S-parameters were fitted in ADS circuit environment and equivalent circuital parameters were extracted. They are

shown in Fig. 6 and result in an inductance value of about 5.8 nH and an equivalent series resistance of 1.6 Ω.

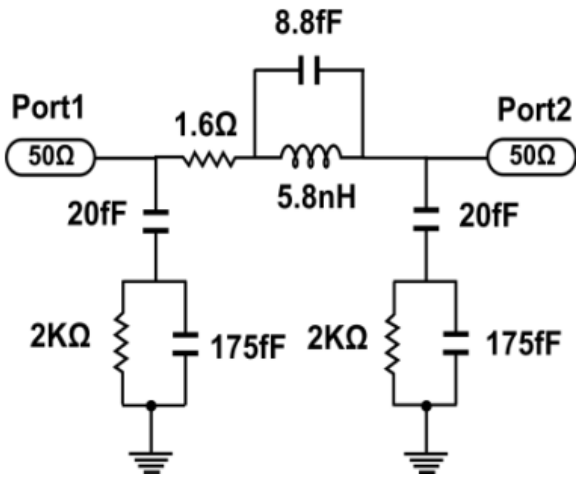


Fig. 6. MEMS spiral inductor: π–model equivalent circuit.

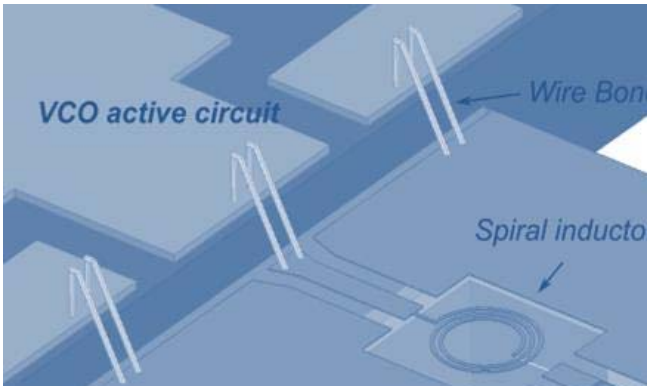
3. Simulation Results of MEMSs Based LC Tank

Finally, the MEMS based series LC resonator was modeled in ANSYS® HFSS full wave environment in the 1 – 5 GHz frequency range. Bonding wires were also modeled to account for the interconnection with the VCO active circuitry. The latter will be fabricated in *surface mount technology* (SMT), on a Roger T–Duroid 4350 substrate, 725 μm thick (Fig. 7).

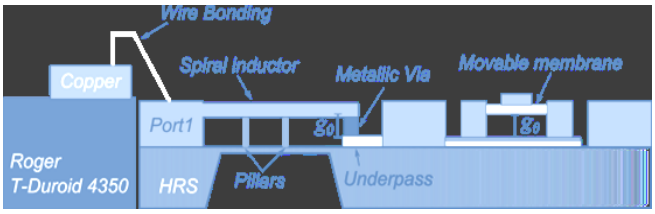
Simulated admittance (real part), as function of the capacitive tuning of the MEMS varicap, is shown in Fig. 8.

The LC resonator shows an overall tuning higher than 60 % in the frequency range 2.15 – 3.85 GHz. Two separate regions of continuous tuning are obtained thanks to the two separate continuous tuning regions of the MEMS varicap. The first one is centered at ~3.65 GHz (WiMAX applications) and allows for a continuous tuning up to 9.5% (3.5–3.85 GHz). The second one allows for a continuous tuning between 2.15 – 2.95 GHz, (30%) ensuring to cover all the frequency bands of WLAN and Bluetooth applications.

At last, the quality factor was computed as in [11], and it is greater than 55 in the frequency range 2.15 – 3.85 GHz.



a)



b)

Fig. 7. MEMS based LC tank: a) 3D–model; b) Cross section.

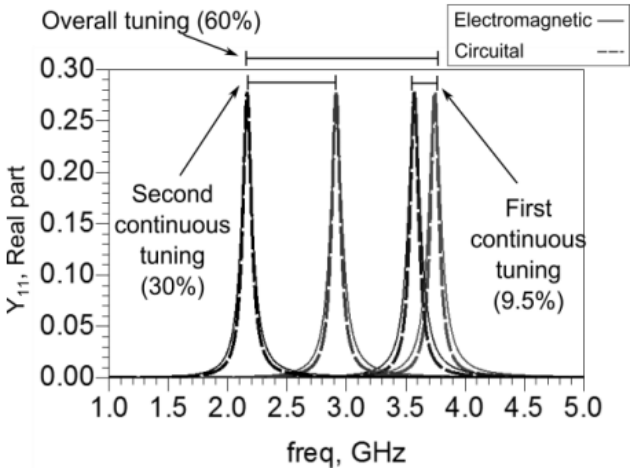


Fig. 8. Simulated full wave (solid line) and circuital (dashed line) admittance (real part) of the MEMS based LC tank.

4. Conclusion

In this paper, the modeling and simulations of a compact multi-band MEMS based LC series resonator has been presented. It is based on a MEMS varicap with an overall capacitive ratio of 5.2 and very high-Q MEMS spiral inductor (~ 60 at 3GHz). The overall size of the device is 2mm × 2mm. The designed resonator shows an overall tuning range of 60% and two separate regions of continuous tuning (9.5% and 30%). Such a LC tank resonators allows the design of VCOs simultaneously operating in the IEEE 802.11b/g (WLAN), IEEE 802.15x (Bluetooth) and IEEE 802.16d (WiMAX) standards. The comparison with the state of the art about MEMS based resonator has been also presented.

References

[1] A.B. BASSAT, A.A. KIDWAI, S. RIVEL R. SADHWANI, *Multi -band Multi-standard Local Oscillator Generation for Direct up/down Conversion Transceiver Architectures Supporting WiFi and WiMax Bands in Standard 45nm CMOS Process*, in IEEE Radio Frequency Integrated Circuits Symposium, pp. 149 – 152, 2010.

[2] Z. XU J. GUO, *Design of Miniature Tri-band Monopole Antenna for WLAN and WiMAX Applications*, in International Conference on Electronic Packaging Technology, 2014.

[3] M. STEER, *Microwave and RF Design: A Systems Approach*, Scitech Pub Inc, 2009.

[4] W.B. KUHN and N.M. IBRAHIM, *Analysis of current crowding effects on multiturn spiral inductors*, IEEE Trans. Microwave Theory & Tech., **49**, pp. 31–38, 2000.

[5] I. BAHL, *Lumped Elements for RF and Microwave Circuits*, Ed. Artech House, 2003.

[6] D.C. EDELSTEIN, M. SOYUER, H.A. AINSPAN and K.A. JENKINS J.N. BURGHARTZ, *RF circuit design aspects of spiral inductors on silicon*, IEEE J. Solid-State Circuits, **33**, pp. 2028 – 2034, 1998.

[7] Y.-S. CHOI and J.-B. YOON, *Experimental analysis of the effect of metal thickness on the quality factor in integrated spiral inductors for RF IC's*, EEE Electron Device Lett., **25**, pp. 76 – 79, 2004.

[8] G.M. REBEIZ, *RF MEMS : Theory, Design, and Technology*, Wiley, 2003.

[9] A. CAZZORLA, P. FARINELLI and R. SORRENTINO, *Double-actuation extended tuning range RF MEMS varactor*, in European Microwave Conference, Paris, 6 – 11 september, 2015.

[10] V. MULLONI, S. COLPO, J. IANNACCI, B. MARGESIN F. GIACOMOZZI and A. FAES, *A Flexible Technology Platform for the Fabrication of RF-MEMS Devices*, in International Semiconductor Conference, Romania, pp. 155 – 158, 2011,

[11] R. SORRENTINO and G. BIANCHI, Microwave and RF Engineering, Wiley, Ed., 2010.

[12] A.Q. LIU, Q.X ZHANG, A.B. YU, *Tunable MEMS LC resonator with large tuning range*, IEEE Electronics Letters, **21**, pp. 855 – 857, 21 July 2005.

[13] J.D. MARTINEZ, M. CHATRAS, A. POTHIER, V.E. BORIA and P. BLONDY, R. STEFANINI, *Ku Band High-Q Tunable Surface-Mounted Cavity Resonator Using RF MEMS Varactors*, IEEE microwave and wireless components letters, **21**(5), 2011.

[14] A. CAZZORLA, P. FARINELLI, R. SORRENTINO, *MEMS based LC tank with extended tuning range for Multi-band applications*, 2015 IEEE 15th Mediterranean Microwave Symposium (MMS), Nov 30 – Dec 2, pp. 1 – 4, 2015.

[15] www.ansys.com

Fabrication and characterization of thermoelectric generators as *in situ* temperature sensor for III-nitride-based power transistors

C. KOLIAKOUDAKIS, A. STAVRINIDIS, A. KOSTOPOULOS, K. TSAGARAKI, K. VAMVOUKAKIS, M. KAYIAMBAKI, V. PRUDKOVSKIY, G. DELIGEORGIS, N. KORNILIOS, G. KONSTANTINIDIS

MRG-IESL-FORTH, Vassilika Vuton, PO Box 1385 Heraklion, Greece
Electrical Engineering Department, Technological Educational Institute of Crete, 71004 Heraklion, Crete, Greece

Abstract. The present work reports on the fabrication and characterization of a thermoelectric generator on the top surface of a power transistor in order to monitor its temperature indirectly through the thermo-generated voltage. The thermoelectric materials used for the generator were n-type Bi/Te and p-type Sb/Te deposited by co-evaporation process. We demonstrated for the first time the use of a thermoelectric generator to monitor the thermal health of III-nitride based power transistors.

Key words: *thermoelectric generator* (TEG), bismuth telluride, antimony telluride, Seebeck effect, temperature monitoring, temperature sensor, *high electron mobility transistor* (HEMT), *monolithic microwave integrated circuits* (MMICs).

1. Introduction

In recent years, III-nitride based *High Electron Mobility Transistors* (HEMTs) have become increasingly popular in the field of high power, high frequency and high temperature microwave systems. High power transistor reliability depends on the maximum operating junction temperature which can exceed 200°C. It is therefore necessary to develop ways to monitor in real time the junction temperature, in order to ensure reliability and device performance. A number of approaches have been used including that of an integrated *Surface Acoustic Wave* (SAW) sensor [1, 2].

Thermoelectric generators (TEGs) are used to convert heat into electricity (Seebeck effect). TEGs can become very attractive because they are compact,

require no moving parts and can be developed at relatively low cost. For temperatures up to 220^0C, *n*-type bismuth telluride (Bi_2Te_3) and *p*-type antimony telluride (Sb_2Te_3) thin films are the most efficient thermoelectric (TE) materials.

This work will report on the integration of a TEG on the top surface of an III-nitride based power HEMT in order to monitor its temperature indirectly through the thermo-generated voltage (HEMT-TEG).

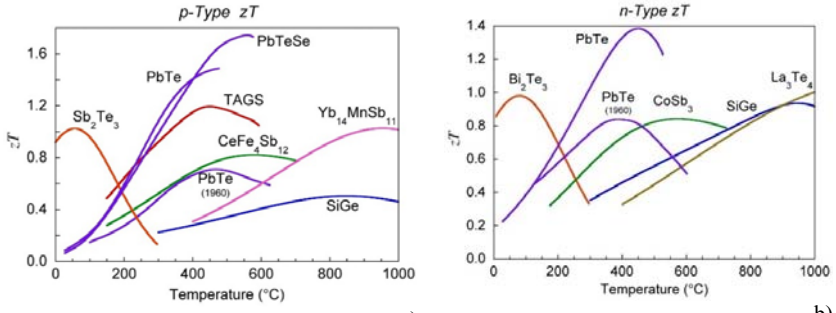
1. Experimental Procedure

In order to establish the correct technological platform for the HEMT-TEG concept, the study focused on three aspects:

1) Growing TE materials of optimum quality, like *n*-type Bi_2Te_3 and *p*-type Sb_2Te_3.
2) Developing optimized fabrication processing modules for the TEG, the HEMT and the HEMT-TEG.
3) Demonstrating for the 1st time the use of a TEG as temperature sensor monitoring the thermal health of III-nitride based power transistors.

Thermoelectric materials and optimization: TE materials can directly convert heat into electrical energy (Seebeck effect) and *vice versa* (Peltier effect). The efficiency of a TE device for electricity generation is given by the figure of merit (ZT) and expressed as $ZT=\frac{\sigma TS^2}{\lambda}$, where Sis the Seebeck coefficient, T is the temperature, σ is the electrical conductivity and λ is the thermal conductivity. To improve the efficiency (ZT), there is a need to simultaneously increase S and σ while reducing the thermal conductance. Since the variables are correlated to each other, increasing the ZT value greater than unity is a complicated task.

From a wide selection of TE materials, Bi_2Te_3 and Sb_2Te_3 compounds are considered good candidates for operation from room temperature up to 200°C. For *p*- and *n*-type materials, ZT values are in the range of 0.8 to 1.1 (Figure 1a and b respectively).



a) b)

Fig. 1. (Color on line). Figure of merit ZT of the most common used TE materials for thermoelectric power generation for (a) p-type and (b) n-type [3].

From published works [4, 5], the Seebeck coefficient and the figure of merit for *n*-type Bi_2Te_3 and *p*-type Sb_2Te_3 are listed below in Table 1.

Table 1. Seebeck coefficient and figure of merit for Bi_2Te_3 and Sb_2Te_3

Material	Seebeck coefficient (μV/K)	Substrate temperature (deposition) T_{sub} (^{0}C)	Electrical conductivity (Ohm*μm)	Figure of merit ($10^{-3}K^{-1}$)
Bi_2Te_3	− 248	270	12.6	2.87
Sb_2Te_3	188	220	12.6	1.63

The Seebeck coefficient of Bi_2Te_3 is negative and the Seebeck coefficient of Sb_2Te_3 is positive. If the two TE materials come into contact and combine to form a junction, then the Seebeck coefficient of the junction willbe.

$$S = S_{BizTea} - S_{SbzTea} = -\frac{436\mu V}{K}$$

In the present work, all depositions were carried out in a high vacuum chamber system (6×10^{-7} Torr), using co-evaporation thermal techniques. Each material evaporation was controlled by the respective "boat" current. In order to calibrate the co-evaporation process and optimize p- and n-type films, co-evaporations following overnight chamber pumping were performed, from high purity (99.999%) Bi, Te and Sb. The influence of the substrate temperature was also examined and optimized in the range between 25 and 150 ^{0}C. The deposition rates of both TE materials were controlled by a single crystal sensor. For the fabrication of Bi_2Te_3 films, the deposition rate of Bi and Te was calibrated between 0.1 − 0.2 nm/s and 0.3 − 0.8 nm/s respectively. A similar procedure was followed for the fabrication of Sb_2Te_3 films, the deposition rate of Sb and Te was calibrated between 0.1 − 0.2 nm/s and 0.3 − 0.8 nm/s respectively.

In order to optimize the deposition parameters and the influence of substrate temperature, the stoichiometric film composition and its structure were studied by *Energy-Dispersive X-ray spectroscopy* (EDX), *Field Emission Scanning Electron Microscope* (FE-SEM) and Hall measurements. In all cases, the Seebeck coefficients were measured at room temperature. One end of the TE material was connected to a heat sink, while the other end to a heater. The Seebeck coefficient of the TE material is a measure of the ratio of a potential difference (ΔV) across the material due to a temperature difference (ΔT). The temperature difference of the two ends is in the range of a few kelvin. The four point probe technique was used to measure the electrical resistivity. The *Power Factor* (PF) was determined using Equation 1, where $\rho$is the electrical resistivity (Ωm).

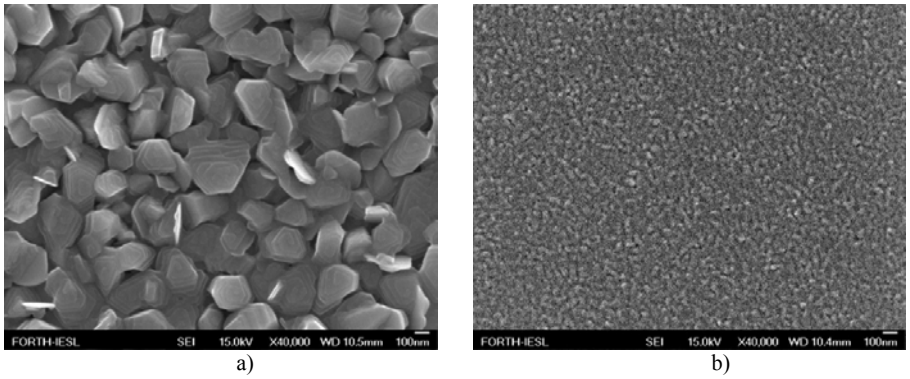
$$PF = S^2 / p \quad (1)$$

All the materials in this study were purchased from Test bourne Ltd. A series of Bi-Teand Sb-Te were fabricated at different flow ratio rates, stoichiometric compositions (at %) and substrate temperatures (T_{sub}) in order to optimize the TE material. Thermoelectric materials were deposited by co-evaporation and patterned by optical lithography using lift-off. Due to lithography, the presence of photoresist on the samples meant that the substrate temperatures during evaporation could not exceed 90^0 C which translates into not using the optimal substrate conditions for the thermoelectric materials growth. All TE films were 300nm thick (+10%). A study has been made of the thermoelectric properties of Bi_xTe_{1-x} and Sb_xTe_{1-x} films, and those that exhibit the best performance for T_{sub} up to 90^0 C are summarized in Table 2.

Table 2. TE properties of selected Bi_2Te_3 and Sb_2Te_3 films

Material	Stoichiometry	Temper. T_{sub} (^{0}C)	S(μV/K)	ρ(Ohm×m)	PF ($WK^{-2}m^{-1}$)
Bi : Te	1 : 2	85	− 52	8.5	0.32
Sb : Te	1 : 3	80	150	15	0.6

SEM images of the Bi-Teand Sb-Te samples were also taken as shown in Figure 2.



a) b)

Fig. 2. SEM images (a) Bi-Te and (b) Sb-Te surfaces.

The morphology of the samples was examined by FE-SEM. Both samples Bi-Te and Sb-Te were consisted of crystal grains, connected to each other. The Bi-Te exhibited grains with diameter up to 400 nm, while the Sb-Te showed much smoother surface with grains diameter up to 70 nm. The thickness of all samples was 300 nm.

HEMT-TEG. The basic processing steps used in fabricating the HEMT-TEG concept are divided into two sequential sub-processes. The first part has to do with

the fabrication of the power transistor (HEMT), while the second with the fabrication of the TEG on the top surface of the HEMT.

The fabrication of the HEMT was optimized on a 3 inch AlGaN/GaN epi-layers on Si substrate. After initial cleaning of the surface, the device fabrication started with the source and drain ohmic contacts, with a source-drain spacing of 5 μm. They were realized by the deposition of Ti/Al/Ni/Au (30/170/40/50 nm) combined with lift-off followed by *Rapid Thermal Annealing* (RTA) at 750 ^{0}C. Following, mesa isolation by reactive-on etching (RIE) in BCl_3/Cl_2 plasma etching was required for device electrical isolation. During this dry etching, part of the wafer was protected from the etchant by photoresist (masking material). After that, a Ni/Au (30/100 nm) gate, with a gate length of 1.5 μm, was formed between the source and the drain ohmic contacts again employing the lift-off approach. After the gate formation, a passivation layer of silicon nitride (Si_3N_4) was grown by *Plasma Enhanced Chemical Vapor Deposition* process (PECVD). The nitridelayer was approximately 200 nm thick and was deposited at 300 ^{0}C. Then a RIE step in SF_6 was performed to locally remove the Si_3N_4 layer. After Si_3N_4 etch, a deposition of Cr/Au (5/300 nm) metal layer and lift-off were used to connect all the gates and drains together with their pads contacts. Finally, the HEMT device was passivated with a second Si_3N_4 200 nm thick, deposited at 300 ^{0}C, in order to protect the top of the power transistor from environmental degradation and to "separate" the HEMT form the "TEG".

After finishing the fabrication of the HEMT, the TEG was fabricated on the top of the second Si_3N_4 passivation layer. N-type Bi_2Te_3 and *p*-type Sb_2Te_3 films 300 nm thick were deposited by thermal co-evaporation techniques. During evaporation the substrate temperature was in the range 85 – 95^{0}C and the working pressure was maintained below 6×10^{-7}Torr. The junctions between the *p* and *n* type layers were fabricated through the deposition of Nickel (Ni) 50 nm employing the lift-off process. The TEG device was finally passivated with a Si_3N_4 200 nm thick, deposited at 150 ^{0}C by PECVD. In order to access the contact pads of the HEMT-TEG, the Si_3N_4 was locally etched using RIE in SF_6.

All 11 photomasks used were designed using the "Clewin" software (Phoenix Technologies). Test structures have also been designed to enable the TE characterization. The detailed manufacturing process flow of the AlGaN/GaN HEMT-TEG and the information about the layers are shown in Figure 3. Phoenix Flow Designer simulates HEMT-TEG components and generates 2D pictures (cross sections).

Two approaches for the HEMT-TEG were designed. The one fabricates the TE modules on the top of the gate of the HEMT (Fig. 4a). Since we had concerns that the TEG could affect the RF performance of the power transistor, we also fabricated the TEG close to the gate (Fig. 4b).

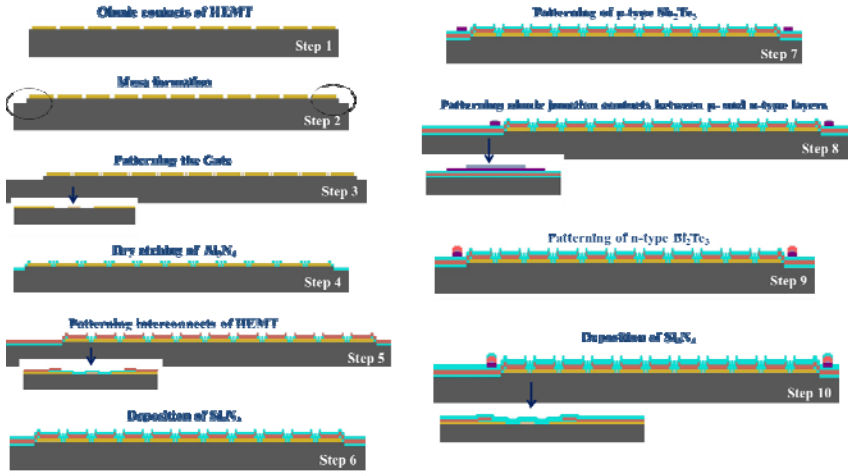


Fig 3. The fabrication process flow of a thermoelectric generator integrated on a AlGaN/GaN HEMT (simulations in Phoenix Flow Designer).

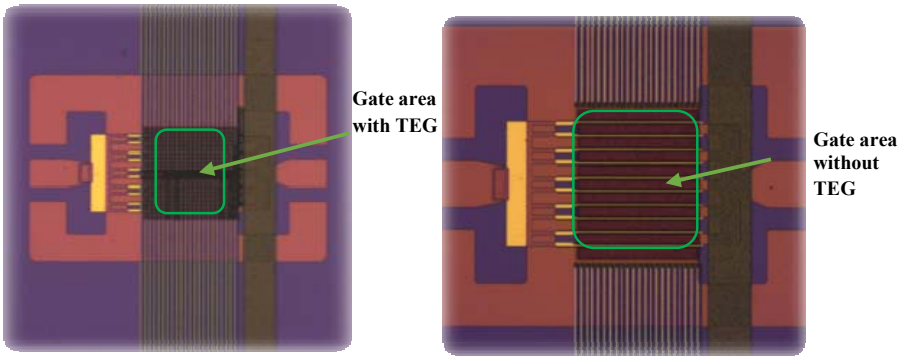


Fig. 4. (Color on line) HEMT-TEG device showing the thermoelectric modules (*p* and *n*-type) fabricated (a) on top of the gate HEMT structure and (b) closed to the gate HEMT structure.

3. Results and Discussion

HEMT-TEG DC & RF characterization: The characterization was performed using a RF probe station connected toa Keithley 2604B and HP8510B

VNA. Initially the transistor was characterized in relation to its DC and RF performance prior to the TEG fabrication. The same set of tests were performed on the transistors after the realization of the TEG. As expected we noticed no difference in the DC performance of the devices.

Figure 5 shows the typical DC behavior of a transistor for different gate voltages. The source-drain current was limited by the VNA current restriction,

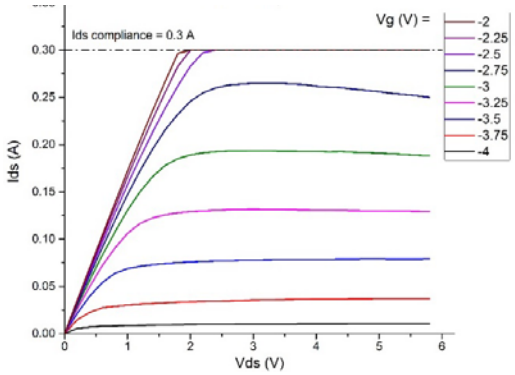


Fig. 5. (Color on line). Typical behavior of the drain current (I_{ds}) as a function of drain voltages (V_{ds}) for different gate voltages (V_g).

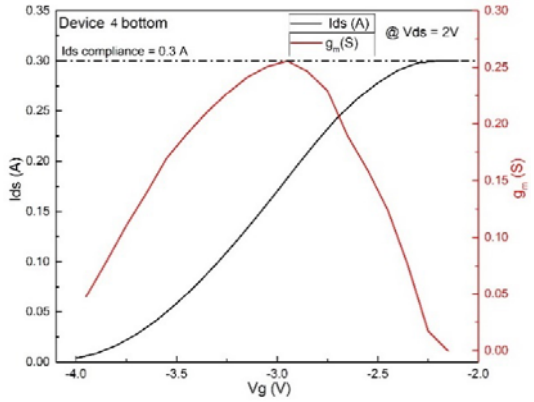


Fig.6. Source-drain current I_{ds} (left axis) and Transconductance (g_m) non normalized to the gate width (right axis) as a function of V_g at constant V_{ds} = 2 V.

which is 0.3 ampere. The power transistor shows a good saturation and pinch-off characteristics. Sweep of the gate voltage at the constant source-drain voltage (Fig. 6) allows us to calculate a transconductance (g_m) from the slope of I_{sd} *vs* V_g, following the formula: $g_m = dI_{ds}/dV_g$

The presence of TEG layers on top of the HEMT (Fig.8) could lead to spurious capacitances that could appear during the RF performance of the device. To clarify this issue we performed RF characterization before and after the fabrication of the TEG. The maximum available power gain (G_{max}) as a function of frequency was obtained form S-parameter measurement at V_{DS}=6V (Fig. 7).

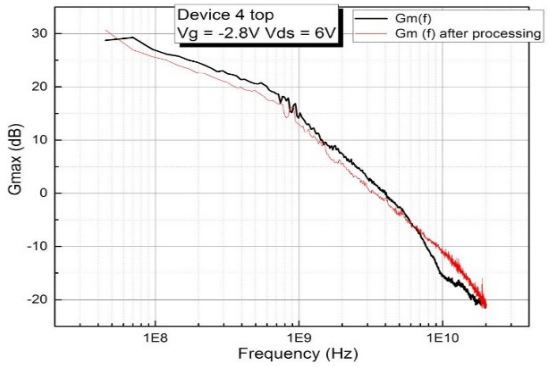


Fig. 7. Maximum available gain (G_{max}) as a function of frequency. The fabrication of TEG layers did not affect the RF behavior of the transistor.

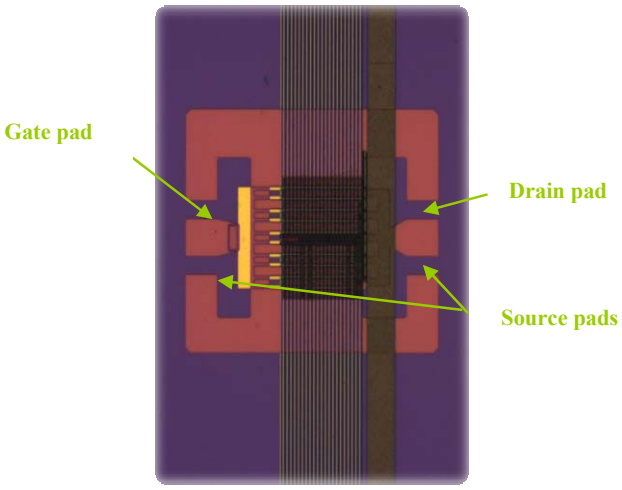


Fig. 8. Finalized HEMT –TEG.

AlGaN/GaN ***HEMT-TEG performance.*** The evaluation of the thermoelectric

generator as *in situ* temperature sensor was performed at room temperature using a Keithley 4200-SCS/F semiconductor characterization system analyzer. The flow of current in the power transistor produces heat at the junctions at the gate regions. Any increase in current flow through the transistor will result in transistor heat up. For AlGaN/GaN HEMTs a typical maximum junction temperature is up to 220^0C (NITRONEX Corp. [6]).The TEG must be triggered by the heat from the transistor and in this way we can monitor the temperature indirectly through the thermo-generated voltage. Several experiments were conducted to measure the thermal voltage of the TEG. The DC I-V measurements employed a drain-source voltage V_{DS} = 0 V to 9 V and a gate-source voltage V_{GS} = 0V. The experimentally measured thermo-generated voltage curves (colored lines) across the TEG as a function of operating time of the transistor, for different drain-source voltages, are presented in Figure 9. The total Seebeck is expressed as

$$S_{total} = S_{BizTea} - S_{SbzTea} \approx -\frac{202\mu V}{^0C} \tag{2}$$

Therefore, the generated thermo-voltage across the TEG (micro generator consists of N = 22 thermocouples) is

$$V_{th} = \left|S_{total}\right| xN\left(thermoelectricpairs\right) \approx \frac{3.5mV}{^0C} \tag{3}$$

The difference between the temperature of the TEG and the air surrounding (ambient temperature) must be taken into account. For all experiments, room temperature is taken to be about 25 ^{0}C. For each drainto source voltage of the

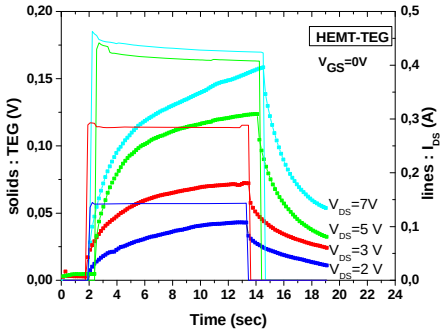


Fig. 9. For V_{GS} = 0V & V_{DS} from 2 to 9 V. TEG's voltage is measured as a function of time (The drain is connected and disconnected manually for each run).

HEMT, the corresponding temperature difference (ΔT) of the TEG is

presented in Table 3.

Table 3. Temperature difference ΔT of the TEG for each drain-source voltage of the HEMT

HEMT V_{DS} (V)	TEG ΔT (^{0}C)
2	42.14
3	59.00
5	73.57
7	77.85

From Table 3, it is clearly shown that for each drain to source voltage, thermo-generated voltage seems to increase exponentially.

Conclusions

The growth of *p*-type (Sb-Te) and *n*-type (Bi-Te) was successfully carried out and the optimum growth parameters were obtained. The stoichiometric ratio for Sb/Te was optimized at 1:3 for *p*-type and the Bi/Te at 1:2 for *n*-type. It is found that the best quality films for *p*-type, S = 150 μV/K, ρ = 15 Ωm and for *n*-type, S = – 52 μV/K, ρ = 8.5 Ωm can be obtained for substrate temperature (T_{sub}) in the range 85 – 90 ^{0}C.

The integration of a TEG on the top surface of the power transistor was designed and manufactured successfully, in order to monitor its temperature indirectly through the thermo-generated voltage. The proof of concept has been experimentally demonstrated for the HEMT-TEG device for the first time. It is concluded that the concept for fabricating the HEMT-TEG device provides a promising procedure as in situ and real time temperature monitoring for power MMICs.

To further improve the efficiency of the TEG sensor we must overcome process constrains and grow TEs at higher T_{sub}

Acknowledgments. The authors wish to thank the project «PROENYL – Advanced Materials for Energy», Action KRIPIS, that was funded by the GSRT, Ministry of Education, Greece.

References

[1] MÜLLER A., GIANGU I., STAVRINIDIS A., STEFANESCU A., STAVRINIDIS G., DINESCU A. KONSTANTINIDIS G. *Sezawa Propagation Mode in GaN on Si Surface Acoustic Wave Type Temperature Sensor Structures Operating at GHz Frequencies*, IEEE Electron Device Letters, **36** Issue: 12 Pages: pp. 1299 – 1302, 2015.

[2] MÜLLER A., KONSTANTINIDIS G., BUICULESCU V., DINESCU A., STAVRINIDIS A., STEFANESCU A., STAVRINIDIS G., GIANGUA I., CISMARU A., MODOVEANU A., *GaN/Si based single SAW resonator temperature sensor operating in the GHz frequency range,* Sensors and Actuators a-Physical, **209** Pages: pp. 115 – 123, 2014.

[3] G. JEFFREY SNYDER, ERIC S. TOBERER, *Complex Thermoelectric Materials*, Nature Materials **7**, pp. 105 – 114, 2008.

[4] L. M. GONCALVES, J. G. ROCHA, C. CUOTO, P. ALPUIM, GAO MIN, D. M. ROWE and J. H. CORREIA, *Fabrication of Flexible Thermoelectric Microcoolers using Planar Thin-Film Technologies*. Journal of Micromechanics and Microengineering, **17**, pp. 168 – 173, 2007.

[5] J. ZHANG, Master Thesis: *Design and Fabrication of On-Chip Cooing Devices Based on the Peltier Effect*, Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, 2010.

[6] NITRONEX CORP, *GaN Essentials AN-012: Thermal Considerations for GaN Technology*, 2008.

Compact Phase Shifting Cell Based on Micro-Strip Slow Wave Lines

M. GASTALDI[1], D. DRAGOMIRESCU[1], A. TAKACS[1], V. ARMENGAUD[2]

[1]LAAS-CNRS, Université de Toulouse, CNRS, (INSA, UPS), Toulouse, France,
[2]CNES RF/HT, 18 Avenue, 31400 Toulouse, France

Abstract. This paper addresses the design, the simulations and the measurements results of an original and compact MMIC phase shifter using micro-strip slow wave lines implemented in a 0.25 µm SiGe BiCMOS process for Ku-band applications. The simulations and the experimental results demonstrate interesting performances compared to classical phase shifter topologies.

1. Introduction

Phase shifters are key components in phase array systems where they achieve beamforming functions. The modern phase array systems developed for telecommunications applications need an increased flexibility and real-time electronic command and control functions. A typical core-chip used for beamforming applications requires a large number of RF phase control points. The performance of such core-chip circuits drives the performance of the final beamforming systems [1]. As example, the classical solution adopted for the beamforming system of the broadcasting satellites involves a 'hybrid' approach. The digital circuits used for command and control functions in the beamforming system are implemented in CMOS based technology while the analog RF functions (phase-shifting and attenuator cells) are mainly implemented in GaAs technology. This 'hybrid' approach increases the complexity, the size and the cost of the beamforming system.

The integration capability on a silicon chip is a key issue allowing a significant footprint reduction beside the low power consumption [2–3]. Consequently, due to the characteristics of Si technologies, a large number of low cost phase shifters have been investigated [4–5].

In this paper, we introduce a novel and original BiCMOS phase shifting cell/topology based on the use of micro-strip *Slow Wave Lines* (SWL). This topology leads to a compact footprint (compared with the footprint of 'classical' topologies [3–5]) while a phase shift below 22.5° is targeted. Also, this topology constitutes a new alternative to other SWL phase shifters [6].

The section II focuses on the proposed topology of the SWL Phase Shifter (SWL PS). The simulated and experimental results obtained for the manufactured 11.25° SWL PS cell are presented in Section III. The performances of the SWL PS cell can be further improved by using body floating or substrate connection techniques as discussed in Section IV.

2. Phase Shifter Design

This phase shifter uses SiGe cold FETs (no bias current) as switches. The phase shift is obtained as a delay between the two signal paths (Fig.1a). The first transmission line is a classical Micro-Strip Line (MSL) and the other transmission is a Shielded Micro-Strip Line (S-MSL). For comparison purposes, the 'classical' topology is represented in Fig 1b. This topology is valid for phase shifter between 90° and 11.25° [4–5].

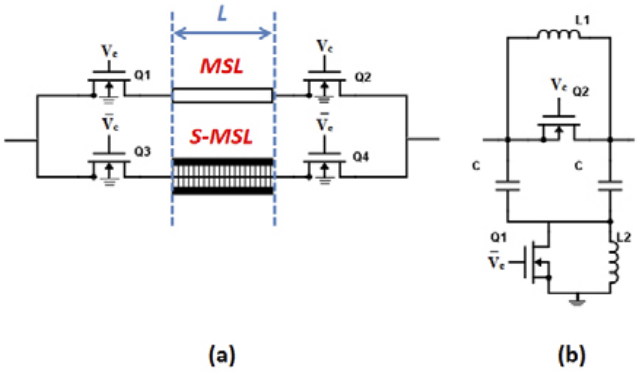


Fig. 1. Proposed phase shifting cell based on SWL: (a) proposed topology, (b) example of the classical topology.

The SWL used to obtain the targeted phase shift is a two layer S-MSL [7] that allows a more compact structure compared to the classical Shielded Coplanar Waveguide (S-CPW). The stack layer of the process is presented in Fig. 2. It offers two thick layers (TM2 and TM1) fitted for carrying the signal and three thin layers (M3, M2 and M1).

As depicted in Fig. 3, the conducting strip is located on the top metal layer (TM2) while the metal strips composing the ground plane are located on the two

layers (TM1 and M3). This disposition of the ground strips on two metal layers prevents the E-field from penetrating the silicon and improves the Q factor [8].

The slow wave line path has been implemented in 0.25µm SiGe BiCMOS process and measured by using a VNA (Anritsu ME7808A).

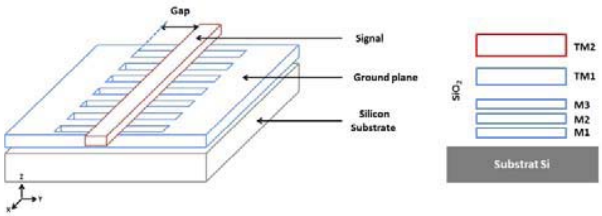


Fig. 2. S-MSL topology and cross section of the BiCMOS process.

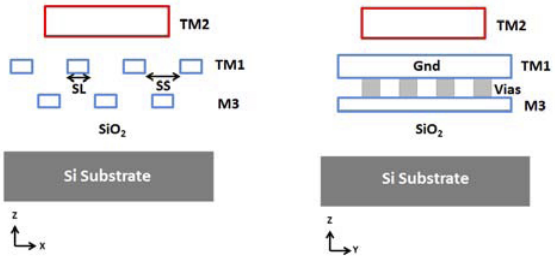


Fig. 3. Cross-section view of the SWL structure.

The S-MSL was obtained after the optimization of the *Strip Length* (SL), the *Strip Spacing* (SS) and the Gap parameters. The experimental results show an improvement of the phase constant by a factor 2.4 compared to a classical MSL (at 15GHz) while the attenuation constant remains almost equivalent [7].

3. Results

The phase shifting cell was fabricated using IHP 0.25µm BiCMOS process. The S-Parameters measurements were performed with a VNA using a standard SOLT calibration procedure. A photo of the dye can be seen on Fig. 4. The size of the phase shifter excluding the pads is 300µm x400µm. In order to simulate the behaviour of the cell, SWLs were electromagnetically simulated on HFSS and then imported on ADS to be combined with the simulation of the transistors. The targeted phase shift was 11.25° (with an authorized deviation of +/– 3°) in the Ku-band: 10.7 – 14.5 GHz. The experimental results for ON (Vc = 2.5 V) and OFF

(Vc = 0 V) states are shows in Fig. 5 (insertion loss) and Fig.6 (return loss). The measurements show important insertion loss for the phase shifting cell. This drawback can be explained by the fact that the bulk of every transistor is directly connected to the ground. Solutions to correct this issue are proposed in section IV. The return losses are under –8.5dB for the targeted band (10 – 15GHz). The difference between the simulations and the measurements can be explained by (i) the impact of the pads (aluminium) that is not taken into account in simulations and (ii) the insertion losses of the transmission lines (especially S-MSL) that are underestimated in HFSS.

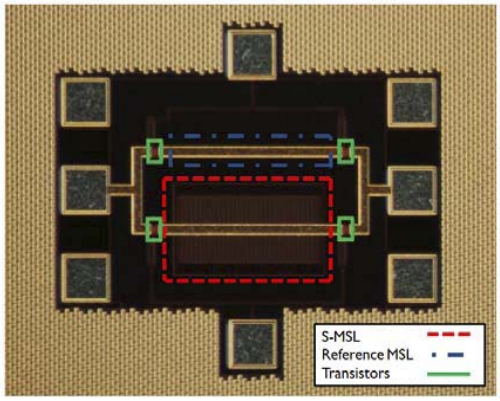


Fig. 4. (Color on line). Photo of the phase shifting cell (250 µm x 400 µm excluding pads).

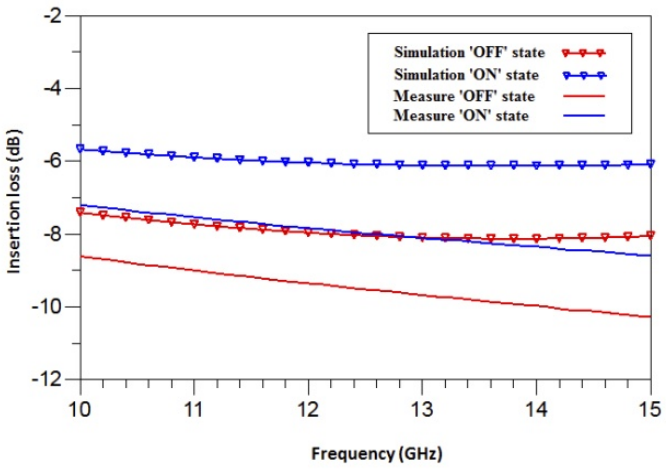


Fig. 5. Insertion loss of the SWL PS for ON/OFF states.

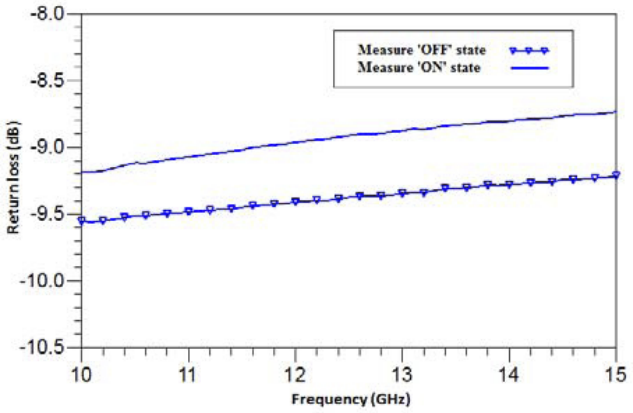


Fig. 6. Return loss of the SWL for the ON/OFF states.

Fig. 7 shows the simulated and measured phase shift of the SWL PS as function of frequency. The differences between the simulations and the measurement are due to the overestimated (in the simulation) phase advance of the SWL line. The FETs being used as switches do not consume DC current (the measured DC current is less than 0.1 μA). Moreover the SWL PS exhibits a quite small linear variation of the phase shift in the targeted frequency band that is very useful from an application point of view.

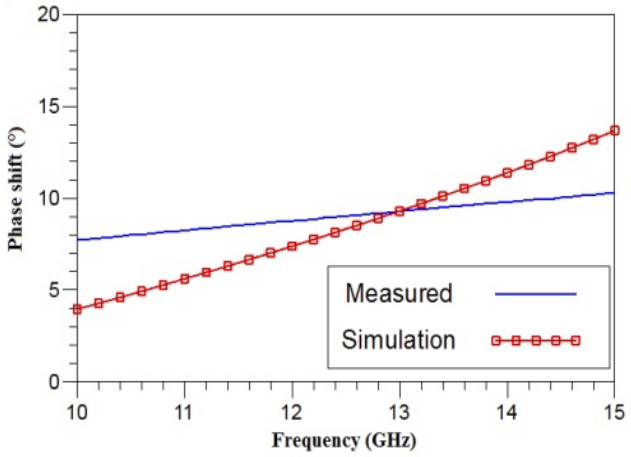


Fig. 7. Phase shift of the SWL PS.

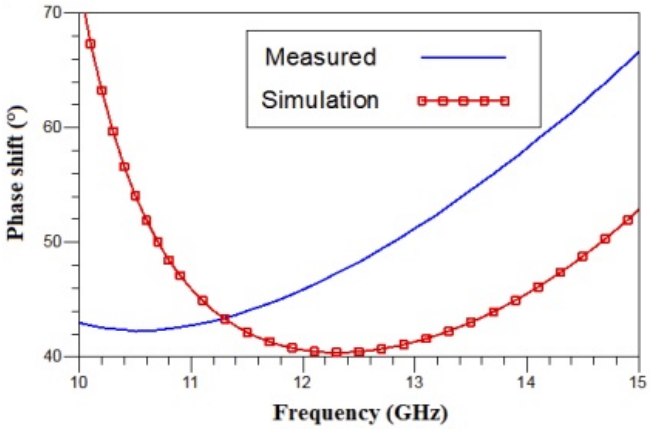


Fig. 8. Phase shift of the 'classical' 45° PS cell.

This cell is even more promising when compared to a 'classical' MMIC phase shifter [2 – 4]. A 11.25° hybrid/classical phase shifter was fabricated on the same run for comparison purposes. Unfortunately this circuit was impacted by a (not detected during design rule check) layout error and the experimental results are not exploitable. However a 45° classical phase shifter cell was fabricated on the same run. The inductors and capacitors values were calculated by the equations given in [4] (Ls = 450 pH, Lp = 1050 pH, C = 105 fF). This cell allows us to check the correlation between the adopted simulation technique under Cadence/ADS and the experimental results. Fig. 8 shows the simulated and the experimental results for the 45° classical PS cell.

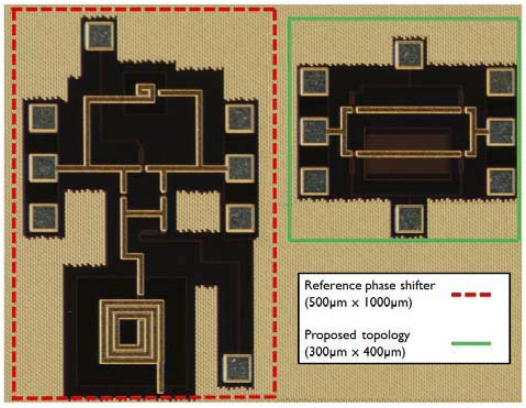


Fig. 9. Size comparison between hybrid topology and SWL based solution

Fig. 9 demonstrates that the SWL-PS topology is more compact as compared with the classical PS topology. The footprint of the SWL-PS is reduced by a factor 3.5 as compared with the footprint of the 'classical' phase shifter when a phase shift of 11.25° is targeted

4. Discussion

As presented in section III, the insertion losses of the phase shifting cell are quite important. Retro-simulations were performed in order to isolate the source of the losses and two solutions are proposed to correct this drawback. It was been found that the main part of the losses was generated by the transistors. The losses added by the switching FETs can be reduced by [8]: (i) connecting the bulk of the FETs to their source (*Bulk Connected to Source*, BCS) and (ii) using the *Body Floating* (BF) technique. BF technique consists of the connecting a 5 kΩ resistor to the bulk of the transistors [8]. BF technique improves also the linearity and the return loss of the cell. The impact of these techniques (BF and BCS) was simulated by using a co-simulation approach. HFSS software was used for the electromagnetic simulation of the S-MSL. The obtained S-parameters (by HFSS simulation) were injected in ADS software that was used for circuit simulation.

Fig.10 (insertion losses) and Fig.11 (return losses) show the experimental and simulated results for the manufactured SWL-PS compared with the simulated results obtained by using the proposed BCS and BF techniques. As depicted in Fig.10 and Fig.11 the use of BF or BCR techniques allows the reduction of the insertion loss and the improvement of the return loss. The BF technique improves also the linearity of the PS cells as represented in Table I (simulation results). The 1dB input compression point is improved with at least 6 dB as function of the topology and of the state (ON/OFF) of the PS.

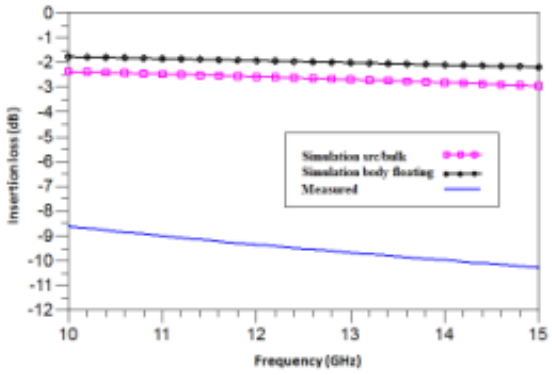


Fig 10. Insertion loss (simulation) of the SWL PS by using BF (diamond marker) and BRC (square marker) techniques compared with the measured results of the fabricated SWL PS (no marker).

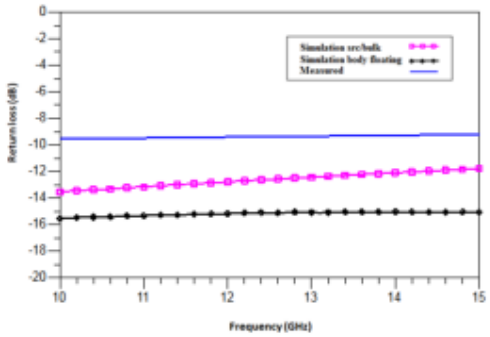


Fig 11. Return loss (simulation) of the SWL PS by using BF (diamond marker) and BRC (square marker) techniques compared with the measured results of the fabricated SWL PS (no marker).

Table. I. 1dB Compression point of the phase shifter cells

	P1dB (dBm)	
	P1dB (dBm):OFF state	***ON state***
PS 45°	3.65	17.9
PS 45° + BF	11.55	24.55
PS 11.25°	3	12
PS 11.25° + BF	11	22
SWL PS	15	19
SWL PS +BF	23	29.2

A new run including an optimized version of the 11.25° SWL-PS cell with pads allowing the access to the bulk is currently in fabrication and more experimental results will be available for the Conference.

5. Conclusion

This paper presents an original and compact phase shifter topology using micro-strip slow wave lines (SWL-PS). The proposed phase shifter exhibits a very low DC power consumption and is a more compact solution compared to the classical hybrid topologies: the footprint is reduced by a factor 3 for a phase shift of 11.25°. This solution remains more compact that the classical topology for a phase shift below 22.5° and constitutes a new alternative to the classical phase shifters. The experimental results for the first manufactured sample based on this innovative SWL-PS show good results in terms of phase shift and return loss. The insertion loss is quite important but as demonstrated by the simulation results these insertion losses can be drastically reduced by using BF or BCS techniques. It was also proven that the BF technique improve the input 1 dB compression point with at least 8 dB for the SWL PS. Moreover the experimental results demonstrate that

the SWL PS topology exhibits a small linear variation of the phase shift over a large frequency bandwidth. This characteristic can be very attractive from critical application (*e.g*. broadcasting satellite telecommunications) where large uplink and downlink bands should be covered by the same beam forming system.

Acknowledgements. The authors would like to acknowledge CNES (French National Spatial Center) for supporting this work by a research grant. They will also like to thank both Thales Alenia Space and CNES for the Ph.D. grant of Mathieu Gastaldi.

References

[1] M. MEGHDADI, M. AZIZI, M. KIANI, A. MEHDI and M. ATARODI, *A 6-Bit CMOS Phase Shifter for S-Band,* in IEEE Transactions on Microwave Theory and Techniques, **58**, no.12, pp.3519-3526, 2010.

[2] M. HANGAI, M. HIEDA, N. YUNOUE, SASAKI, YOSHINOBU, M. MIYAZAKI, *S- and C-Band Ultra-Compact Phase Shifters Based on All-Pass Networks,* in Microwave Theory and Techniques, IEEE Transactions on , **58**, no.1, pp. 41-47, 2010.

[3] YOUNSUB NOH, MANSEOK UHM, INBOK YOM, *Ku-band Up- converter Multi-function MMIC using 0.25 µm SiGe BiCMOS Technology*, Microwave Conference, 2009. APMC 2009. Asia Pacific, pp.1164-1167, 2009.

[4] B-W. MIN, G.M. REBEIZ, *Single-Ended and Differential Ka-Band BiCMOS Phased Array Front-Ends*, IEEE Journal of Solid-State Circuits, vol.**43**, no.10, pp.2239-2250, 2008.

[5] I. KALYONCU, E. OZEREN, M. KAYNAK, Y. GURBUZ, *A 4-bit SiGe passive phase shifter for X-band phased arrays*, Radio and Wireless Symposium (RWS), 2013 IEEE, pp.310-312, 20-23, 2013.

[6] M. BAKRI-KASSEM, MANSOUR, RAAFAT;S. SAFAVI-NAEINI, *Novel millimeter-wave slow-wave phase shifter using MEMS technology,* Microwave Integrated Circuits Conference (EuMIC), 2011 European, pp.518-521, 2011.

[7] M. GASTALDI, D. DRAGOMIRESCU, A. TAKACS, V. ARMENGAUD, S. ROCHETTE, *Micro-strip slow wave line for phase shifting cells*, Electronics Letters, **51**, no.20, pp.1589-1591, 2015.

[8] T. DINC, I. KALYONCU,Y. GURBUZ, *An X-Band Slow Wave T/R Switch in 0.25 um SiGe BiCMOS*, IEEE Transactions on Circuits and Systems II: Express Brief, **61**, no.2, pp.65-69, 2014.

This volume is promoted by the Commission: *Science and Technology of Microsystems* of the Romanian Academy with the technical and financial support of the National Institute for Research and Development in Microtechnologies (IMT Bucharest, http://www.imt.ro). The volume is part of the *Micro and Nanoengineering series*, (coordinator – Professor Dan Dascalu, member of the Romanian Academy).